

SNx4LS245 Octal Bus Transceivers With 3-State Outputs

1 Features

- 3-State Outputs Drive Bus Lines Directly
- PNP Inputs Reduce DC Loading on Bus Lines
- Hysteresis at Bus Inputs Improves Noise Margins
- Typical Propagation Delay Times Port to Port, 8 ns

2 Applications

- Building Automation
- Electronic Point of Sale
- Factory Automation and Control
- Test and Measurement

3 Description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

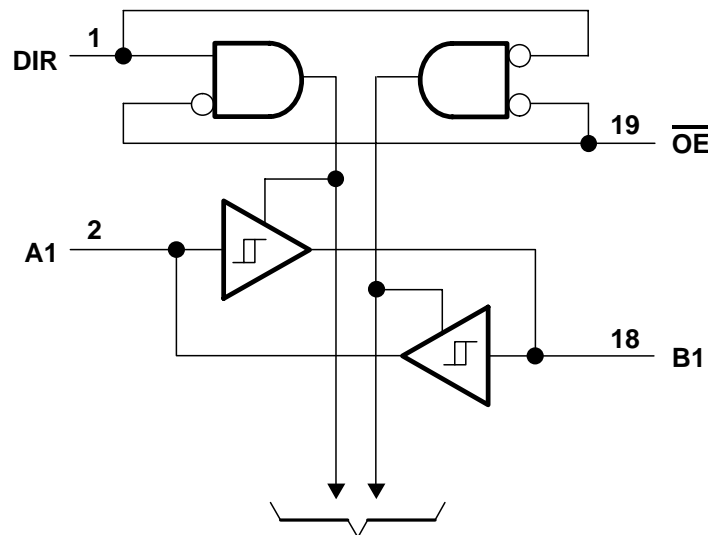
The SNx4LS245 devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can disable the device so that the buses are effectively isolated.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN54LS245J	CDIP (20)	24.20 mm x 6.92 mm
SN54LS245W	CFP (20)	7.02 mm x 13.72 mm
SN54LS245FK	LCCC (20)	8.89 mm x 8.89 mm
SN74LS245DB	SSOP (20)	7.20 mm x 5.30 mm
SN74LS245DW	SOIC (20)	12.80 mm x 7.50 mm
SN74LS245N	PDIP (20)	24.33 mm x 6.35 mm
SN74LS245NS	SO (20)	12.60 mm x 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



To Seven Other Channels

Copyright © 2016, Texas Instruments Incorporated



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

Table of Contents

1 Features	1	9.3 Feature Description	8
2 Applications	1	9.4 Device Functional Modes	8
3 Description	1	10 Application and Implementation	10
4 Revision History	2	10.1 Application Information	10
5 Device Comparison Table	3	10.2 Typical Application	10
6 Pin Configuration and Functions	3	11 Power Supply Recommendations	12
7 Specifications	4	12 Layout	12
7.1 Absolute Maximum Ratings	4	12.1 Layout Guidelines	12
7.2 ESD Ratings	4	12.2 Layout Example	12
7.3 Recommended Operating Conditions	4	13 Device and Documentation Support	13
7.4 Thermal Information	4	13.1 Related Links	13
7.5 Electrical Characteristics	5	13.2 Receiving Notification of Documentation Updates	13
7.6 Switching Characteristics	5	13.3 Community Resource	13
7.7 Typical Characteristics	6	13.4 Trademarks	13
8 Parameter Measurement Information	7	13.5 Electrostatic Discharge Caution	13
9 Detailed Description	8	13.6 Glossary	13
9.1 Overview	8	14 Mechanical, Packaging, and Orderable Information	13
9.2 Functional Block Diagram	8		

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

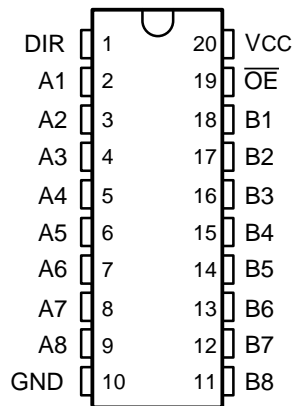
Changes from Revision A (February 2002) to Revision B	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Deleted <i>Ordering Information</i> table; see POA at the end of the data sheet	1
• Changed $R_{\theta JA}$ values in <i>Thermal Information</i> table: 70 to 91.7 for DB package, 58 to 79 for DW package, 69 to 46.1 for N package, and 60 to 74.2 for NS package	4

5 Device Comparison Table

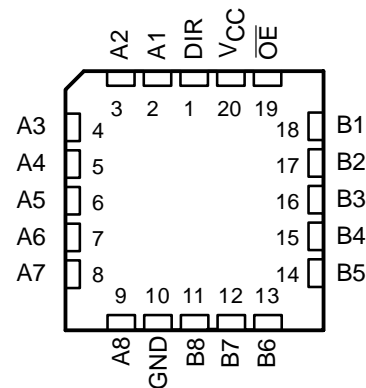
TYPE	I_{OL} (SINK CURRENT)	I_{OH} (SOURCE CURRENT)
SN54LS245	12 mA	-12 mA
SN74LS245	24 mA	-15 mA

6 Pin Configuration and Functions

J, W, DB, DW, N, or NS Package
20-Pin CDIP, CFP, SSOP, SOIC, PDIP, or SO
Top View



FK Package
20-Pin LCCC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	DIR	I	Controls signal direction; Low = Bx to Ax, High = Ax to Bx
2	A1	I/O	Channel 1, A side
3	A2	I/O	Channel 2, A side
4	A3	I/O	Channel 3, A side
5	A4	I/O	Channel 4, A side
6	A5	I/O	Channel 5, A side
7	A6	I/O	Channel 6, A side
8	A7	I/O	Channel 7, A side
9	A8	I/O	Channel 8, A side
10	GND	—	Ground
11	B8	O/I	Channel 8, B side
12	B7	O/I	Channel 7, B side
13	B6	O/I	Channel 6, B side
14	B5	O/I	Channel 5, B side
15	B4	O/I	Channel 4, B side
16	B3	O/I	Channel 3, B side
17	B2	O/I	Channel 2, B side
18	B1	O/I	Channel 1, B side
19	\overline{OE}	I	Active low output enable; Low = all channels active, High = all channels disabled (high impedance)
20	V _{CC}	—	Power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage		7	V
V_I	Input voltage ⁽¹⁾		7	V
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) All voltage values are with respect to GND.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	SN54LS245	4.5	5	5.5	V
		SN74LS245	4.75	5	5.25	
I_{OH}	High-level output current	SN54LS245			-12	mA
		SN74LS245			-15	
I_{OL}	Low-level output current	SN54LS245			12	mA
		SN74LS245			24	
T_A	Operating free-air temperature	SN54LS245	-55		125	°C
		SN74LS245	0		70	

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SNx4LS245							UNIT	
	J (CDIP)	W (CFP)	FK (LCCC)	DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SO)		
	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	N/A	N/A	N/A	91.7	79.0	46.1	74.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.3 ⁽²⁾	70.1 ⁽²⁾	46.7 ⁽²⁾	53.1	44.4	32.1	40.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.9 ⁽²⁾	109.5 ⁽²⁾	45.6 ⁽²⁾	46.8	46.9	27.0	41.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	N/A	N/A	N/A	18.9	18.0	17.6	16.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	N/A	N/A	N/A	46.4	46.3	26.9	41.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15.9 ⁽²⁾	13.0 ⁽²⁾	6.7 ⁽²⁾	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

(2) MIL-STD-883 for R_{th-JC} JEDEC JESD51 for R_{th-JB} (body not contact PCB)

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IH}	High-level input voltage			2			V
V _{IL}	Low-level input voltage	SN54LS245				0.7	V
		SN74LS245				0.8	
V _{IK}	Input clamp voltage	V _{CC} = MIN,	I _I = -18 mA			-1.5	V
Hysteresis (V _{T+} - V _{T-})		A or B	V _{CC} = MIN	0.2	0.4		V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = V _{IL(max)} V _{IH} = 2 V,	I _{OH} = -3 mA	2.4	3.4		V
			I _{OH} = MAX	2			
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL(max)}	I _{OL} = 12 mA			0.4	V
			I _{OL} = 24 mA	SN74LS245			
I _{OZH}	Off-state output current, high-level voltage applied	V _{CC} = MAX, OE at 2 V	V _O = 2.7 V			20	μA
I _{OZL}	Off-state output current, low-level voltage applied	V _{CC} = MAX, OE at 2 V	V _O = 0.4 V			-200	μA
I _I	Input current at maximum input voltage	A or B DIR or OE	V _{CC} = MAX	V _I = 5.5 V		0.1	mA
				V _I = 7 V		0.1	
I _{IH}	High-level input current	V _{CC} = MAX,	V _{IH} = 2.7 V			20	μA
I _{IL}	Low-level input current	V _{CC} = MAX,	V _{IL} = 0.4 V			-0.2	mA
I _{OS}	Short-circuit output current ⁽²⁾	V _{CC} = MAX		-40		-225	mA
I _{CC}	Supply current	Total, outputs high	V _{CC} = MAX Outputs open		48	70	mA
		Total, outputs low			62	90	
		Outputs at high Z			64	95	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

7.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 45 pF, R _L = 667 Ω		8	12	ns
t _{PHL}	Propagation delay time, high- to low-level output			8	12	
t _{PZL}	Output enable time to low level	C _L = 45 pF, R _L = 667 Ω		27	40	ns
t _{PZH}	Output enable time to high level			25	40	
t _{PLZ}	Output disable time from low level	C _L = 5 pF, R _L = 667 Ω		15	25	ns
t _{PHZ}	Output disable time from high level			15	28	

7.7 Typical Characteristics

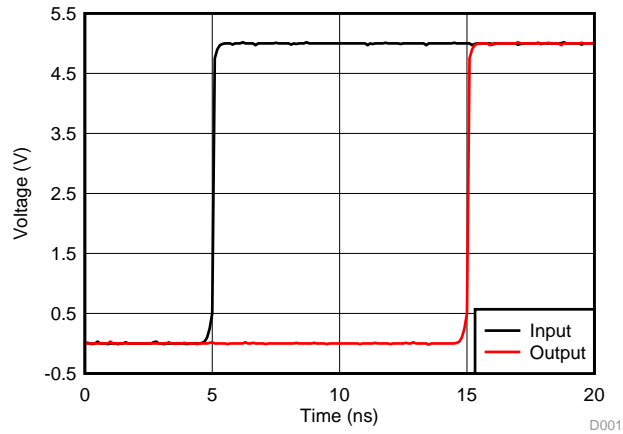
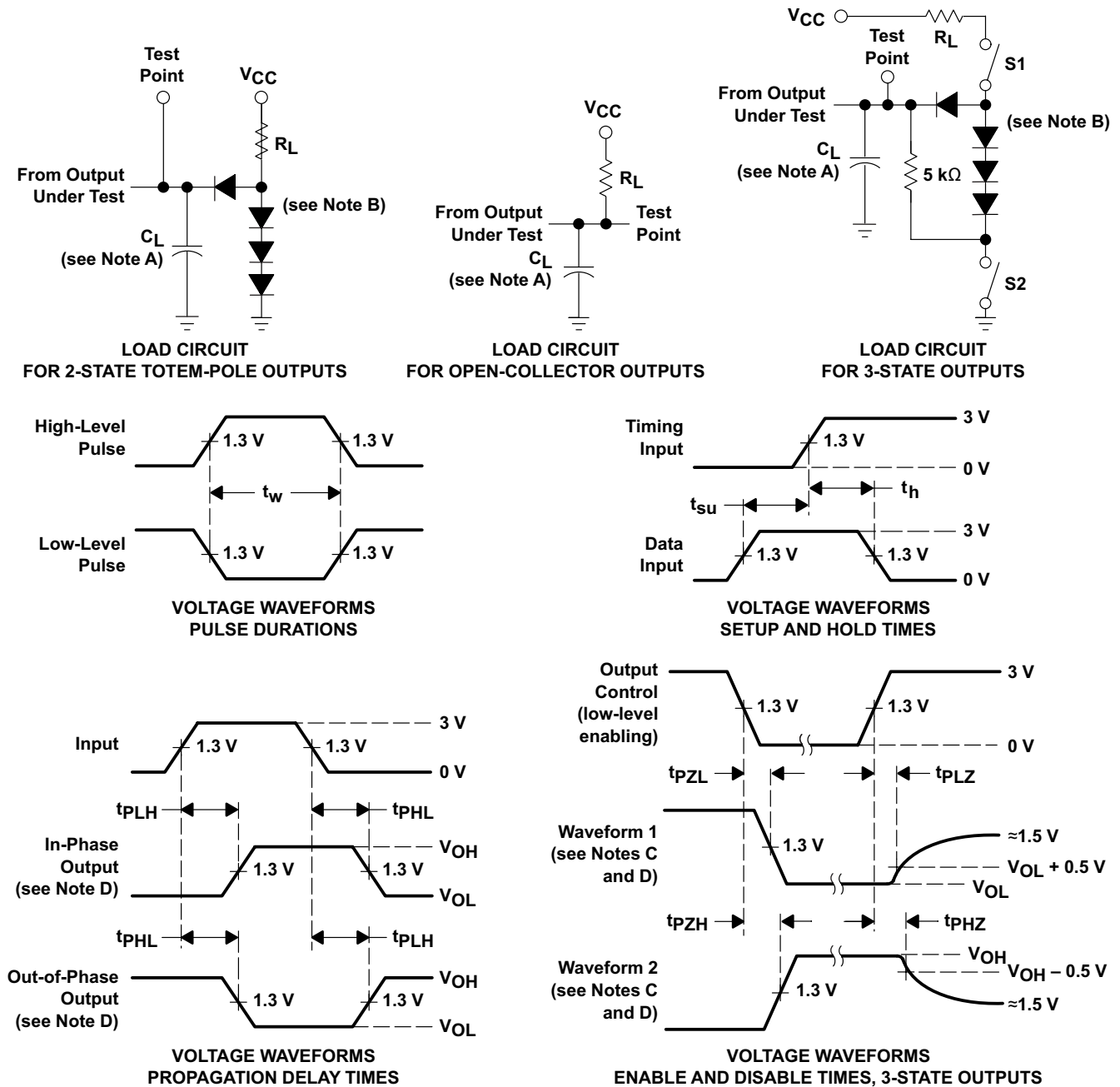
 $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 45\text{ pF}$, $R_L = 667\ \Omega$


Figure 1. Simulated Propagation Delay From Input to Output

8 Parameter Measurement Information



- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
 E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
 F. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$, $t_r \leq 1.5$ ns, $t_f \leq 2.6$ ns.
 G. The outputs are measured one at a time with one input transition per measurement.

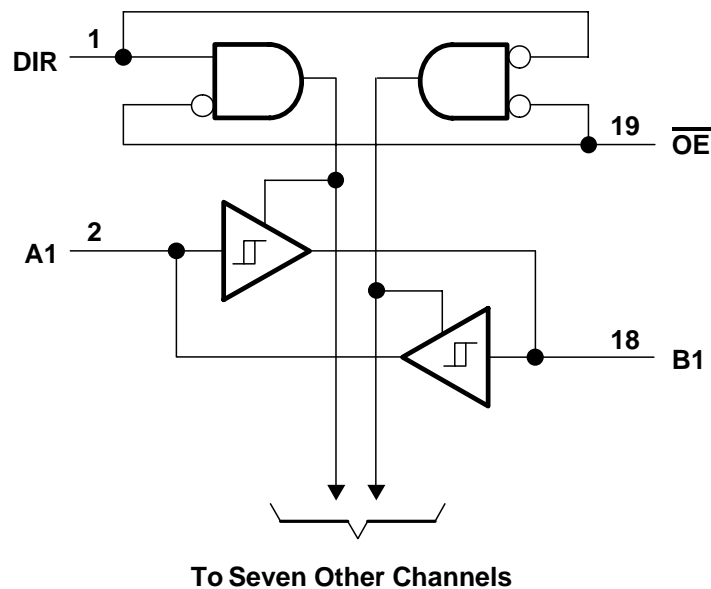
Figure 2. Load Circuits and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SNx4LS245 uses Schottky transistor logic to perform the standard '245 transceiver function. This standard logic function has a common pinout, direction select pin, and active-low output enable. When the outputs are disabled, the A and B sides of the device are effectively isolated.

9.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

Figure 3. Logic Diagram (Positive Logic)

9.3 Feature Description

9.3.1 3-State outputs

The 3-state outputs can drive bus lines directly. All outputs can be put into high impedance mode through the \overline{OE} pin.

9.3.2 PNP Inputs

This device has PNP inputs which reduce dc loading on bus lines.

9.3.3 Hysteresis on Bus Inputs

The bus inputs have built-in hysteresis that improves noise margins.

9.4 Device Functional Modes

The SNx4LS245 performs the standard '245 logic function. Data can be transmitted from A to B or from B to A depending on the DIR pin value, or the A and B sides can be isolated from one another by setting the \overline{OE} pin HIGH.

Table 1. Function Table

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

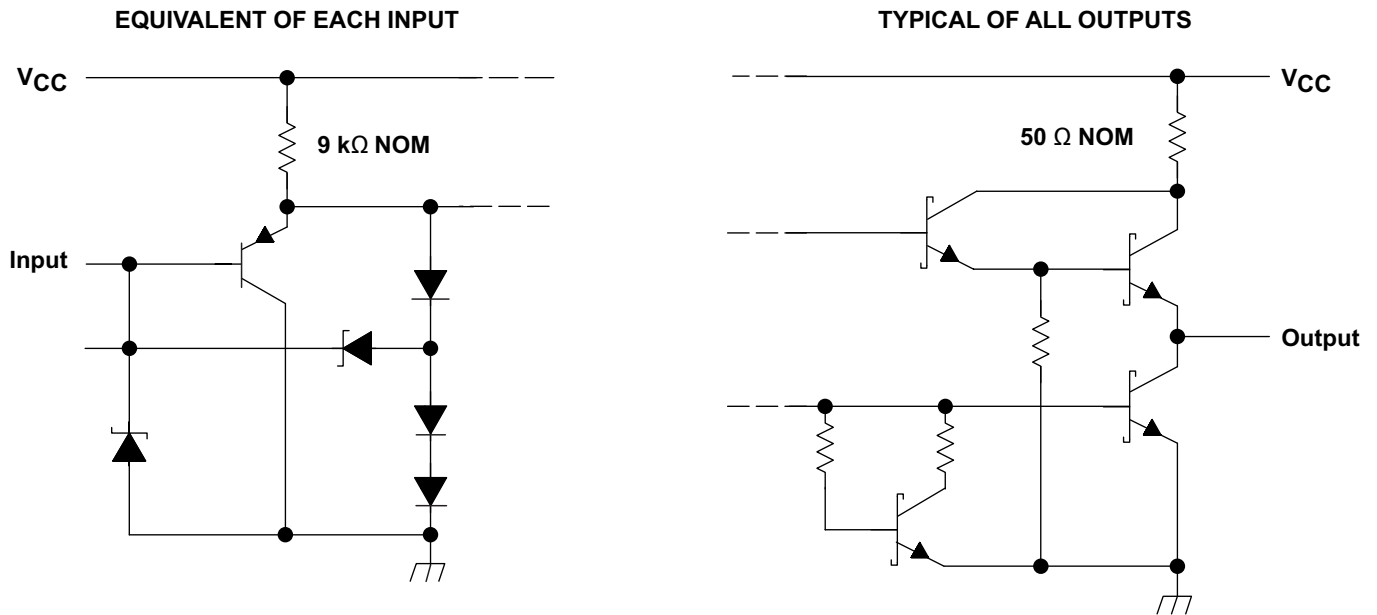


Figure 4. Schematics of Inputs and Outputs

10 Application and Implementation

NOTE

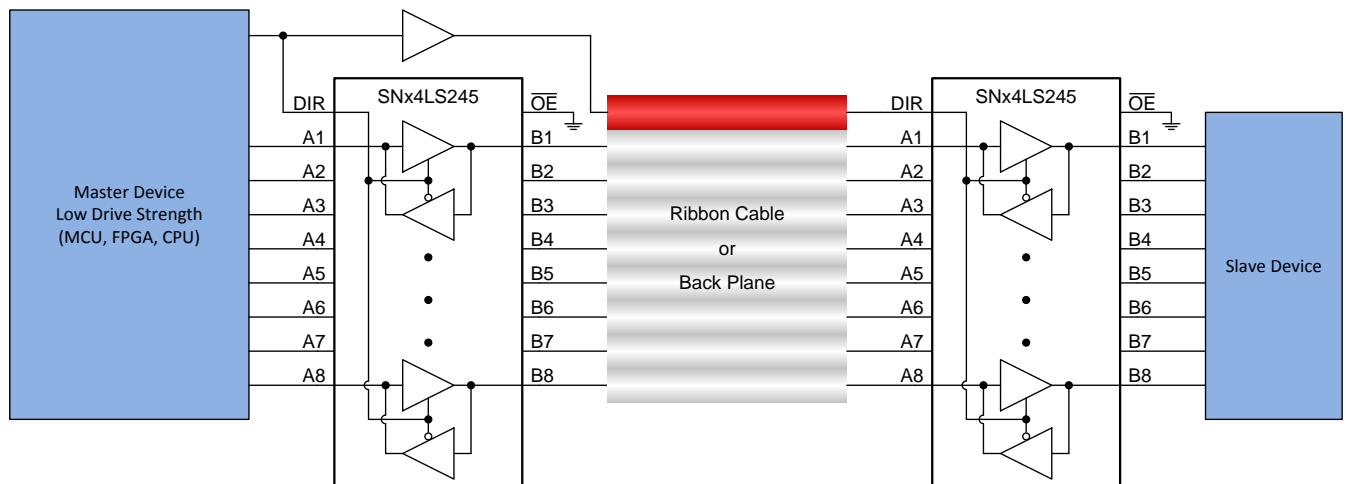
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SNx4LS245 is commonly used to drive ribbon cables or back plane busses. It allows isolation from the bus when necessary, and increases drive strength on the bus.

10.2 Typical Application

Figure 5 shows the SNx4LS245 wired up as a permanently enabled data bus transceiver for both a master and slave device communicating over a ribbon cable or back plane.



Copyright © 2016, Texas Instruments Incorporated

Figure 5. SNx4LS245 Being Used to Communicate Over a Ribbon Cable or Back Plane

10.2.1 Design Requirements

This device uses Schottky transistor logic technology. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

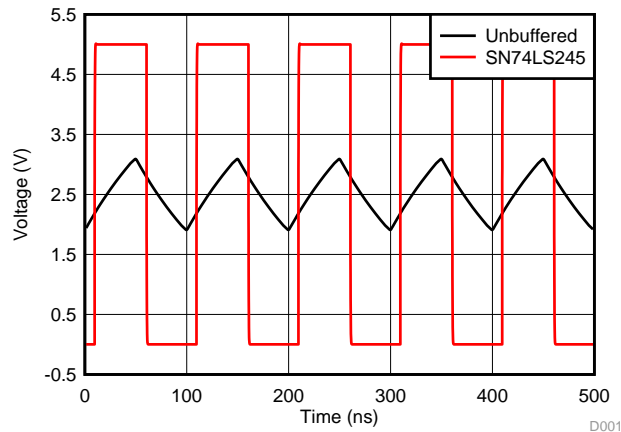
10.2.2 Detailed Design Procedure

- Power Supply
 - Each device must maintain a supply voltage between 4.5 V and 5.5 V
- Inputs
 - Input signals must meet the V_{IH} and V_{IL} specifications in [Electrical Characteristics](#)
 - Inputs leakage values (I_I , I_{IH} , I_{IL}) from [Electrical Characteristics](#) must be considered
- Outputs
 - Output signals are specified to meet the V_{OH} and V_{OL} specifications in [Electrical Characteristics](#) as a minimum (the values could be closer to V_{CC} for high signals or GND for low signals)
 - TI recommends maintaining output currents as specified in [Recommended Operating Conditions](#)
 - The part can be damaged by sourcing or sinking too much current. See [Electrical Characteristics](#) for details.

Typical Application (continued)

10.2.3 Application Curve

It is common to see significant losses in ribbon cables and back planes. Figure 6 shows a simplified simulation of a ribbon cable from a 5-V, 10-MHz low-drive strength source. It shows the difference between an input signal from a weak driver like an MCU or FPGA compared to a strong driver like the SN74LS245 when measured at the distant end of the cable. By adding a high-current drive transceiver before the cable, the signal strength can be significantly improved, and subsequently the cable can be longer.



Unbuffered line is directly connected to low current source, SN74LS245 line is buffered through the transceiver. Both signals are measured at the distant end of the ribbon cable. **Input signal is not shown.**

Figure 6. Simulated Outputs From Ribbon Cable With a 5-V, 10-MHz Source

11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in [Recommended Operating Conditions](#). Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- μF bypass capacitor. If there are multiple V_{CC} pins, TI recommends a 0.01- μF or 0.022- μF bypass capacitors for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. Two bypass capacitors of value 0.1 μF and 1 μF are commonly used in parallel. For best results, install the bypass capacitor(s) as close to the power pin as possible.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices, inputs must not be left floating. In many applications, some channels of the SNx4LS245 are unused, and thus must be properly terminated. Because each transceiver channel pin can be either an input or an output, they must be treated as both when being terminated. Ground or V_{CC} (whichever is more convenient) can be used to terminate unused inputs; however, each unused channel should be terminated to the same logic level on both the A and B side. For example, in [Figure 7](#) unused channels 4, 5, 6, and 7 are terminated correctly with both sides connected to the same voltage, while channel 8 is terminated incorrectly with each side being tied to a different voltage. The $\overline{\text{OE}}$ input is also unused in this example, and is terminated directly to ground to permanently enable all outputs.

12.2 Layout Example

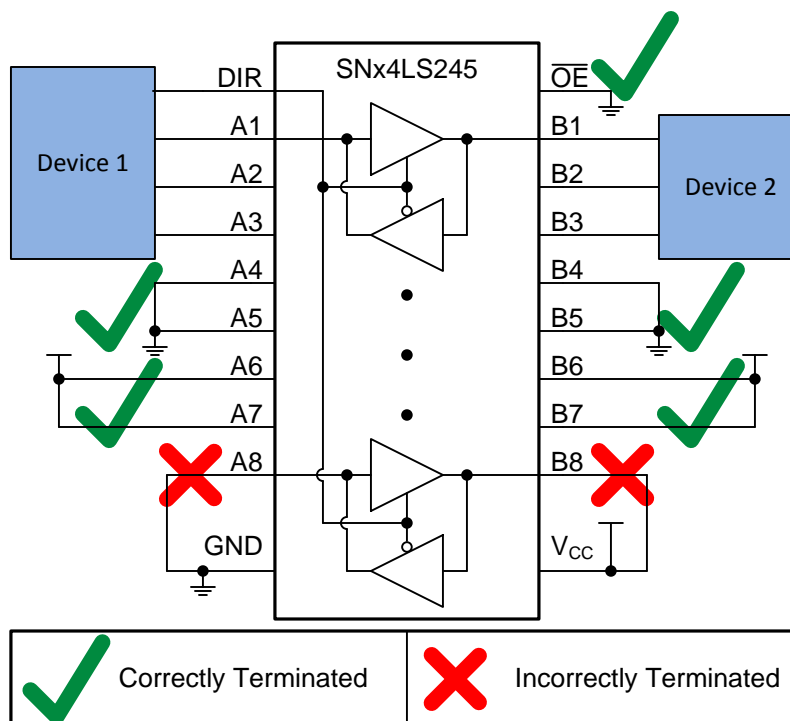


Figure 7. Example Demonstrating How to Terminate Unused Inputs and Channels of a Transceiver

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LS245	Click here	Click here	Click here	Click here	Click here
SN74LS245	Click here	Click here	Click here	Click here	Click here

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8002101VSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8002101VS A SNV54LS245W	Samples
80021012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	80021012A SNJ54LS 245FK	Samples
8002101SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8002101SA SNJ54LS245W	Samples
JM38510/32803B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32803B2A	Samples
JM38510/32803BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32803BRA	Samples
JM38510/32803BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32803BSA	Samples
M38510/32803B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32803B2A	Samples
M38510/32803BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32803BRA	Samples
M38510/32803BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32803BSA	Samples
SN54LS245J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS245J	Samples
SN74LS245DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS245	Samples
SN74LS245DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS245	Samples
SN74LS245DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS245	Samples
SN74LS245DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS245	Samples
SN74LS245N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS245N	Samples
SN74LS245NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS245N	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS245NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS245	Samples
SNJ54LS245FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	80021012A SNJ54LS 245FK	Samples
SNJ54LS245J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS245J	Samples
SNJ54LS245W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8002101SA SNJ54LS245W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LS245, SN54LS245-SP, SN74LS245 :

- Catalog: [SN74LS245](#), [SN54LS245](#)

- Military: [SN54LS245](#)

- Space: [SN54LS245-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS245DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LS245DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS245NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS245DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74LS245DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS245NSR	SO	NS	20	2000	367.0	367.0	45.0

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

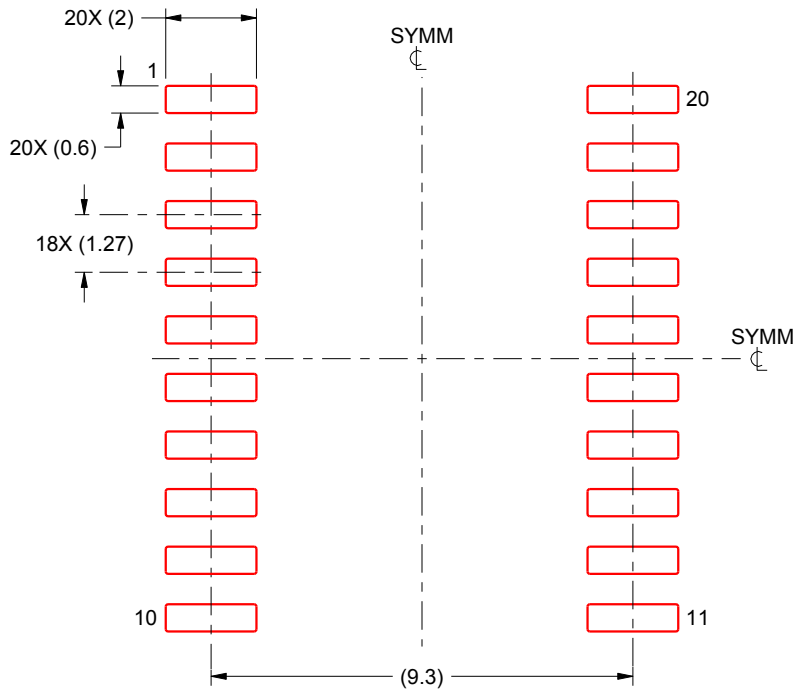
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.