Electrically Erasable PROM

FEATURES

- 250 ns Access Time
- Fast Write Cycle Times
  - —16-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 2.6 Sec. Typical
  - —Effective Byte Write Cycle Time of 300 μs Typical
- $\overline{\text{DATA}}$ Polling
  - —Allows User to Minimize Write Cycle Time
- High Reliability
  - —Endurance: 10,000 Writes Per Byte
  - —Data Retention: 100 Years
- Simple Byte and Page Write
  - —Single TTL Level $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

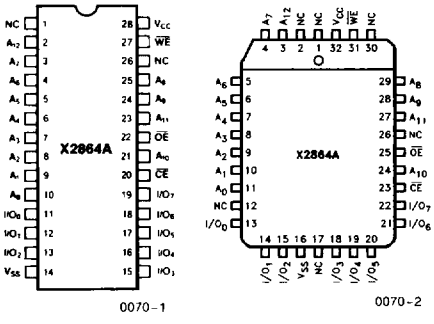
DESCRIPTION

The Xicor X2864A is a 8K x 8 E²PROM, fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories. The X2864A features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

The X2864A supports a 16-byte page write operation, effectively providing a 300 μs/byte write and enabling the entire memory to be written in less than 2.6 seconds. The X2864A also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E²PROMs are designed and tested for applications requiring extended endurance and data retention. Endurance is specified as 10,000 cycles per byte minimum and data retention is specified as 100 years minimum. Refer to Xicor reliability reports RR-520 and RR-515 for details of endurance and data retention characteristics.

PIN CONFIGURATIONS



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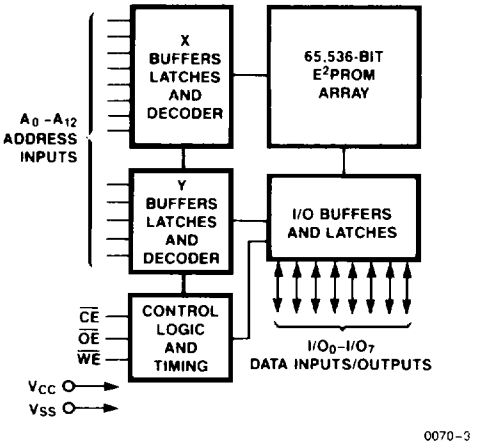
PIN NAMES

A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X2864A ..... −10°C to +85°C
X2864AI ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2864A T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2864AI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	X2864A Limits		X2864AI Limits		Units	Test Conditions
		Min.	Max.	Min.	Max.		
I_{CC}	V_{CC} Current (Active)		140		140	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{SB}	V_{CC} Current (Standby)		60		70	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{LI}	Input Leakage Current		10		10	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10		10	μA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(3)	Input Low Voltage	−1.0	0.8	−1.0	0.8	V	
V_{IH}(3)	Input High Voltage	2.0	V_{CC} +0.5	2.0	V_{CC} +1.0	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		2.4		V	I_{OH} = −400 μA

TYPICAL POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(2)	Power-Up to Read Operation	1	ms
t_{PUW}(2)	Power-Up to Write Operation	5	ms

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) This parameter is periodically sampled and not 100% tested.
(3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units	Conditions
Endurance	10,000		Cycles/Byte	Xicor Reliability Report RR-520
Data Retention	100		Years	Xicor Reliability Report RR-515

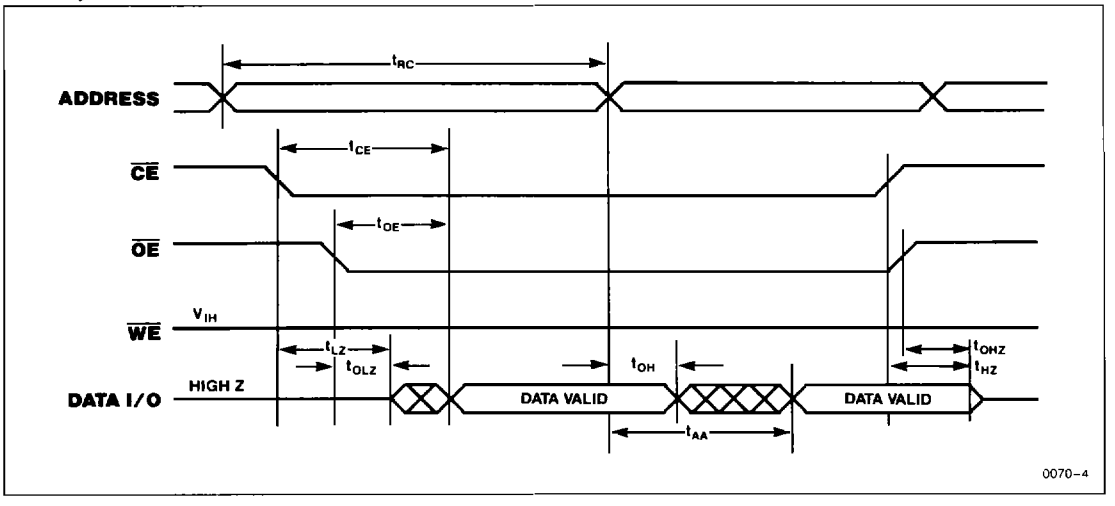
A.C. CHARACTERISTICS

X2864A T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2864AI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	X2864A-25 X2864AI-25		X2864A X2864AI		X2864A-35 X2864AI-35		X2864A-45 X2864AI-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	250		300		350		450		ns
t_{CE}	Chip Enable Access Time		250		300		350		450	ns
t_{AA}	Address Access Time		250		300		350		450	ns
t_{OE}	Output Enable Access Time		100		100		100		100	ns
t_{LZ}(4)	Chip Enable to Output in Low Z	10		10		10		10		ns
t_{HZ}(4)	Chip Disable to Output in High Z	10	60	10	80	10	80	10	100	ns
t_{OLZ}(4)	Output Enable to Output in Low Z	10		10		10		10		ns
t_{OHZ}(4)	Output Disable to Output in High Z	10	60	10	80	10	80	10	100	ns
t_{OH}	Output Hold from Address Change	10		10		10		10		ns

Read Cycle

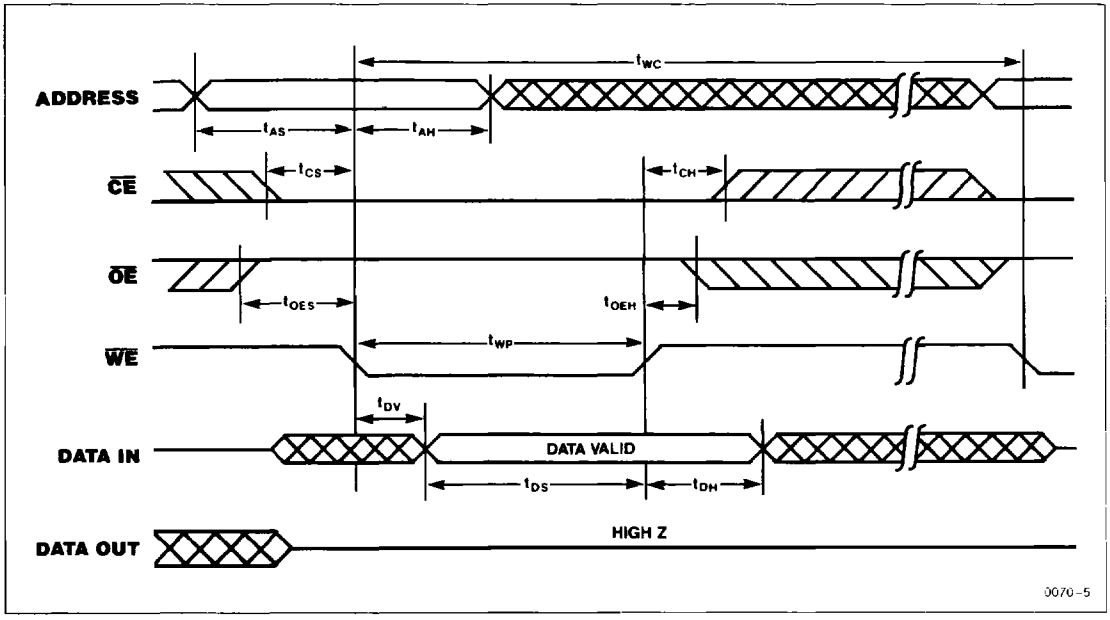


Note: (4) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min., t_{OHZ} min., t_{LZ} min. and t_{OLZ} min. are periodically sampled and are not 100% tested.

Write Cycle Limits

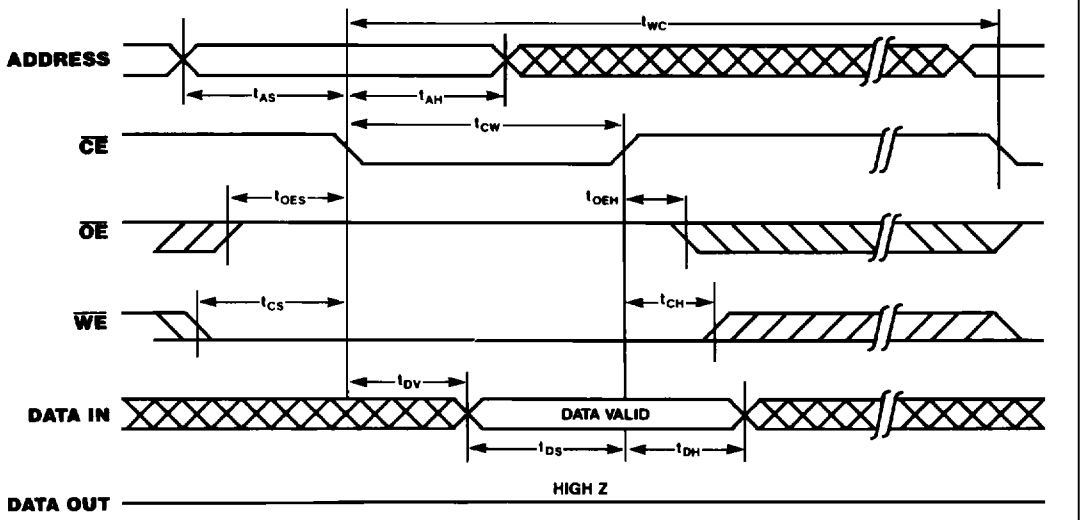
Symbol	Parameter	Min.	Max.	Units
t_{WC}(5)	Write Cycle Time		10	ms
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time	200		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	$\overline{CE}$ Pulse Width	150		ns
t_{OES}	$\overline{OE}$ High Setup Time	10		ns
t_{OEH}	$\overline{OE}$ High Hold Time	10		ns
t_{WP}	$\overline{WE}$ Pulse Width	150		ns
t_{WPH}	$\overline{WE}$ High Recovery	50		ns
t_{DV}	Data Valid		300	ns
t_{DS}	Data Setup	100		ns
t_{DH}	Data Hold	20		ns
t_{DW}	Delay to Next Write	500		μs
t_{BLC}	Byte Load Cycle	3	40	μs

$\overline{WE}$ Controlled Write Cycle

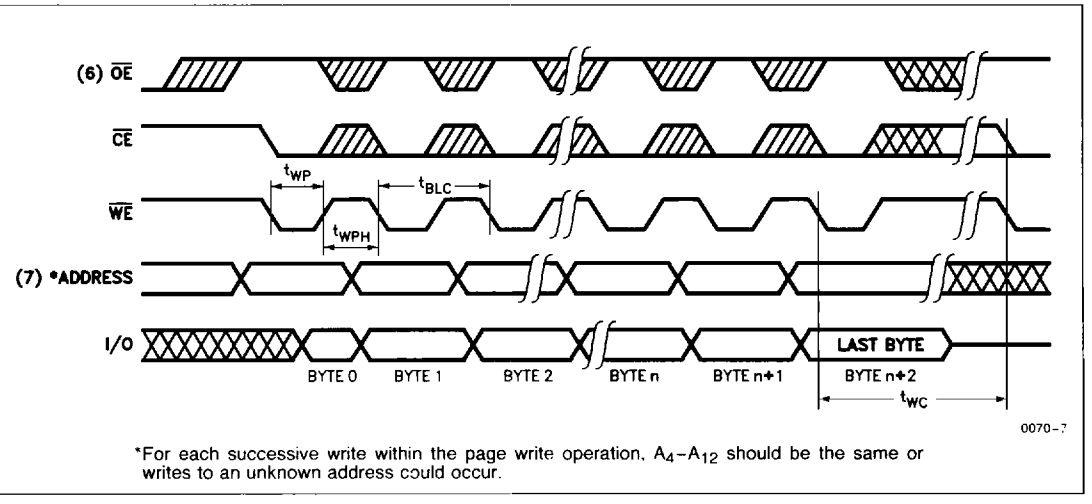


Note: (5) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

$\overline{CE}$ Controlled Write Cycle



Page Mode Write Cycle

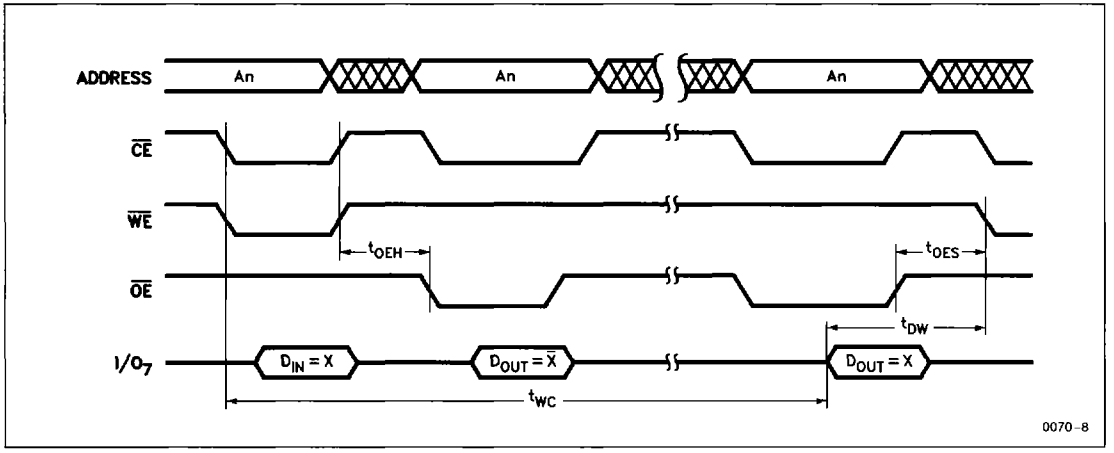


*For each successive write within the page write operation, A_4–A_{12} should be the same or writes to an unknown address could occur.

Notes: (6) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(7) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(8)



Note: (8) A polling operation by definition is a read cycle and therefore subject to read cycle timings.

PIN DESCRIPTIONS

Addresses (A_0–A_{12})
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)
The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)
Data is written to or read from the X2864A through the I/O pins.

Write Enable ($\overline{WE}$)
The Write Enable input controls the writing of data to the X2864A.

DEVICE OPERATION

Read
Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write
Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X2864A supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation
The page write feature of the X2864A allows the entire memory to be written in 2.6 seconds. Page write allows two to sixteen bytes of data to be consecutively written to the X2864A prior to the commencement of the internal programming cycle. The destination addresses for a page write operation must reside on the same page; that is, A_4 through A_{12} must not change.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to fifteen bytes in the same manner as the first byte was written. Each successive byte write cycle must begin within 20 μs of the falling edge of $\overline{WE}$ of the preceding cycle. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 20 μs the internal automatic programming cycle will commence.

$\overline{DATA}$ Polling
The X2864A features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X2864A, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

WRITE PROTECTION
There are three features that protect the nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse of less than 20 ns will not initiate a write cycle.
- V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$3V, typically.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CE}$ HIGH during power-on and power-off, will inhibit inadvertent writes.

SYSTEM CONSIDERATIONS

Because the X2864A is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

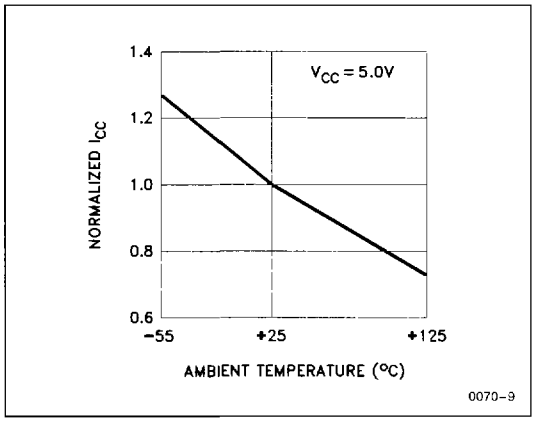
Because the X2864A has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

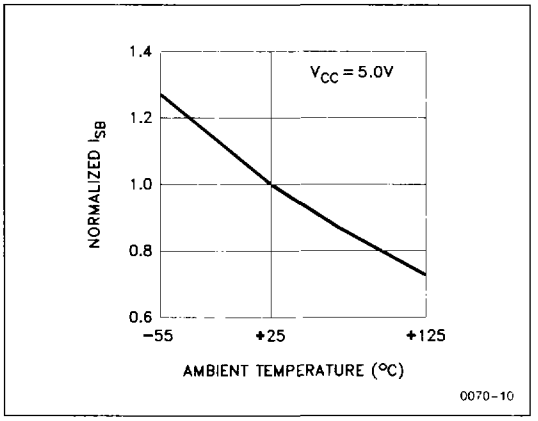
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

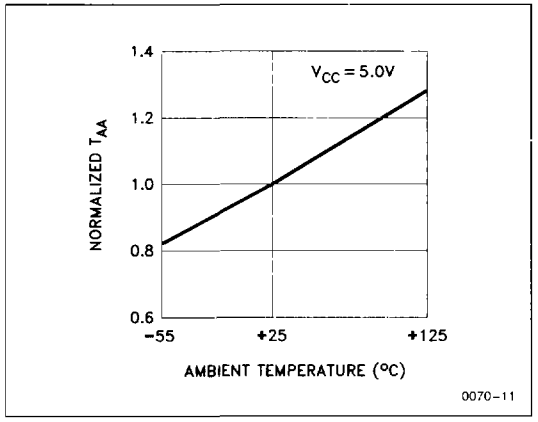
Normalized Active Supply Current vs. Ambient Temperature



Normalized Standby Supply Current vs. Ambient Temperature



Normalized Access Time vs. Ambient Temperature



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