Winbond Clock Generator
W83194BR-655/W83194BG-655
For SiS 655 Chipsets

Date: Feb/14/2006 Revision: 1.0

W83194BR-655 Data Sheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1					All of the versions before 0.50 are for internal use.
2	n.a.	10/11/2003	0.5	n.a.	First published preliminary version.
3	20	12/18/03	0.6	n.a.	Correction IC version,
4		2/14/2006	1.0	1.0	Update on Web and PB free part
5					
6					
7					
8					
9					
10					

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

Table of Content-

1. GENERAL DESCRIPTION

The W83194BR-655 is a Clock Synthesizer for SIS 655 chipset with 964 South Bridge. W83194BR-655 provides all clocks required for high-speed microprocessor and provides step-less frequency programming and 32 different frequencies of CPU, PCI, and AGP clocks setting, support two ZCLK clock outputs; all clocks are externally selectable with smooth transitions.

The W83194BR-655 provides I^2C serial bus interface to program the registers to enable or disable each clock outputs and provides -0.5% and +/-0.25% center type spread spectrum or programmable S.S.T. scale to reduce EMI.

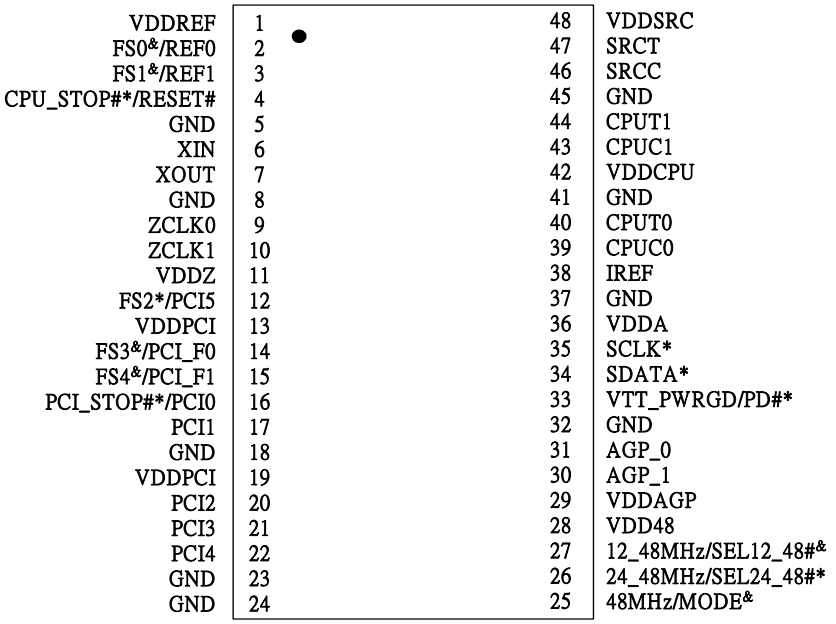
The W83194BR-655 also has watchdog timer to support auto-reset when systems hanging caused by improper frequency setting.

The W83194BR-655 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply.

2. PRODUCT FEATURES

- 2 pairs current mode Differential clock outputs for CPU
- 1 pairs current mode Differential clock output for SRC.
- 2 3.3V ZCLK clock outputs
- 2 AGP clock outputs
- 8 PCI synchronous clocks
- 1 24_48Mhz clock output for super I/O.
- 1 12/48 MHz clock output
- 2 14.318MHz REF clock outputs.
- ZCLK/AGP/PCI clock out supports synchronous and asynchronous mode
- Smooth frequency switch with selections from 100 to 274MHz
- Step-less frequency programming
- I^2C 2-Wire serial interface and support byte read/write and block read/write.
- -0.5% and +/- 0.25% center type spread spectrum
- Programmable S.S.T. scale to reduce EMI
- Programmable registers to enable/stop each output and select modes
- Programmable clock outputs Skew control
- Watch Dog Timer and RESET# output pins
- 48-pin SSOP package

3. PIN CONFIGURATION

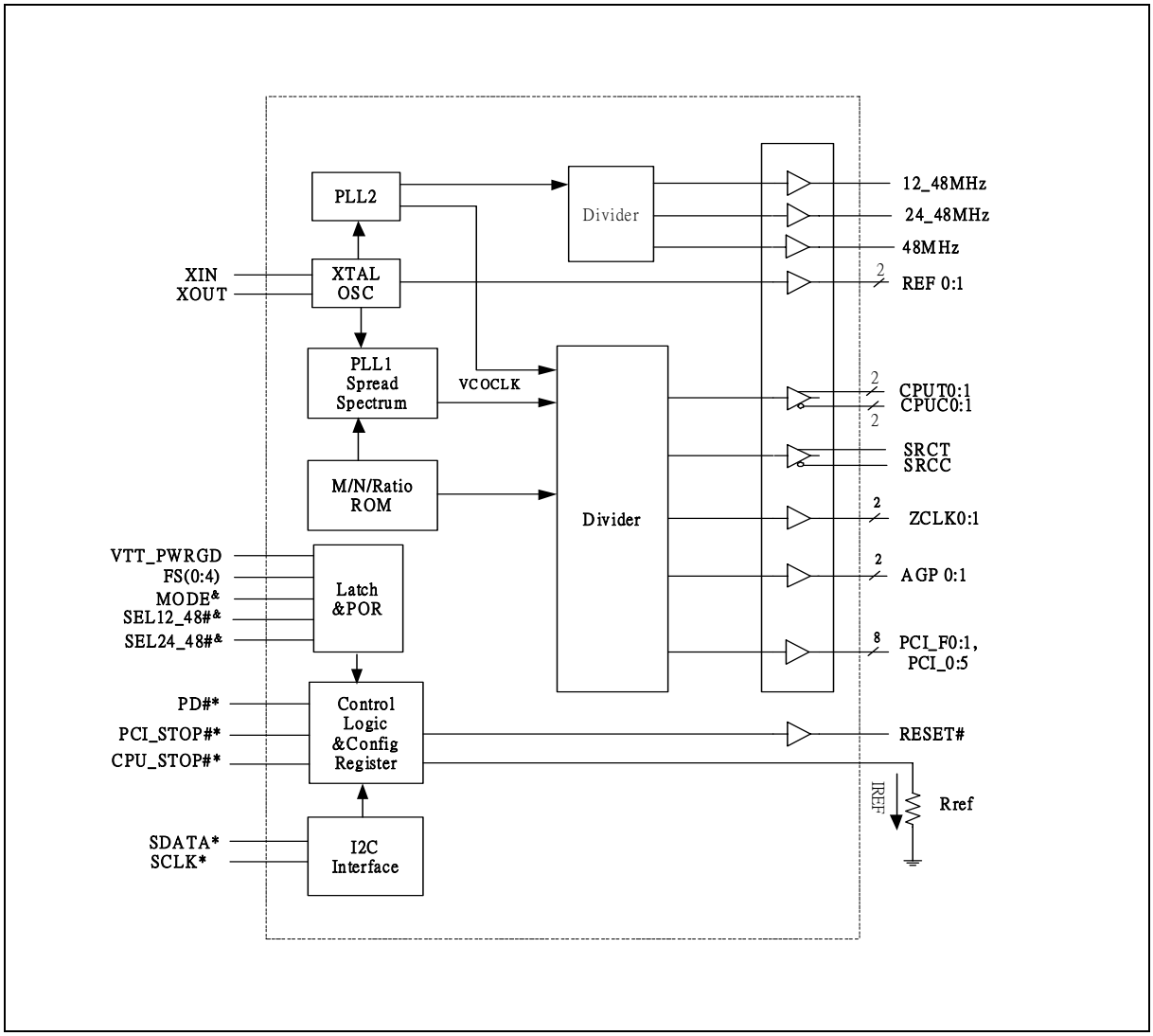


#: Active low

*: Internal pull up resistor 120K to VDD

&: Internal Pull-down resistor 120K to GND

4. BLOCK DIAGRAM



5. PIN DESCRIPTION

BUFFER TYPE SYMBOL	DESCRIPTION
IN	Input
IN_{tp120k}	Latched input at power up, internal 120kΩ pull up.
IN_{td120k}	Latched input at power up, internal 120kΩ pull down.
OUT	Output
OD	Open Drain
#	Active Low
*	Internal 120kΩ pull-up
&	Internal 120 kΩ pull-down

5.1 Crystal I/O

PIN	PIN NAME	TYPE	DESCRIPTION
6	XIN	IN	Crystal input with internal loading capacitors (18pF) and feedback resistors.
7	XOUT	OUT	Crystal output at 14.318MHz nominally with internal loading capacitors (18pF).

5.2 CPU, AGP, ZCLK and PCI Clock Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
40,39,44,43	CPUT0: 1 CPUC0: 1	OUT	Current mode differential clock outputs for CPU & Chipset
47,47	SRCT, SRCC	OUT	Current mode differential clock outputs, For SRC
31,30	AGP_0: 1	OUT	3.3V AGP clock outputs.
9,10	ZCLK0: 1	OUT	3.3V ZCLK clock outputs, For MuTIOL bus.
14	PCI_F0	OUT	3.3V PCI free running clock output.
	FS3&	IN_{td120k}	Latched input for FS3 at initial power up for H/W selecting the output frequency. This is internal 120K pull down.
15	PCI_F1	OUT	3.3V PCI free running clock output.
	FS4&	IN_{td120k}	Latched input for FS4 at initial power up for H/W selecting the output frequency, This is internal 120K pull down.
16	PCI0	OUT	3.3V PCI clock output.
	PCI_STOP#*	IN_{tp120k}	Active low, Stop all PCI clock output besides the free running clocks, Select by power up latched MODE#=1,This is internal 120K pull up.
17,20,21,22	PCI [1:4]	OUT	Low skew (< 250ps) 3.3V PCI clock outputs.
12	PCI5	OUT	3.3V PCI clock output.
	FS2*	IN_{tp120k}	Latched input for FS2 at initial power up for H/W selecting the output frequency, This is internal 120K pull up.

5.3 Fixed Frequency Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
2	REF0	OUT	14.318MHz output.
	FS0[&]	IN_{td120k}	Latched input for FS0 at initial power up for H/W selecting the output frequency. This is internal 120K pull down.
3	REF1	OUT	14.318MHz output.
	FS1[&]	IN_{td120k}	Latched input for FS1 at initial power up for H/W selecting the output frequency. This is internal 120K pull down.
25	48MHz	OUT	48MHz clock output
	MODE[&]	IN_{td120k}	Latched input for pin 4,16 at initial power up selecting the default=0 pin 4 is RESET# and pin16 is PCICLK0, MODE=1, pin 4 is CPU_STOP#* and pin 16 is PCISTOP#. This is internal 120KΩ pull down.
27	12_48MHz	OUT	12MHz or 48MHz(default) clock output select by power up latched SEL12_48#
	SEL12_48#[&]	IN_{td120k}	Latched input for 12_48MHz at initial power up selecting the 0=48MHz clock output, 1=12MHz clock output. This is internal 120KΩ pull down.
26	24_48MHz	OUT	24MHz (default) or 48MHz clock output select by power up latched SEL24_48#,
	SEL24_48#*	IN_{tp120k}	Latched input for 24_48MHz at initial power up selecting the 0=48MHz clock output, 1=24MHz clock output. This is internal 120KΩ pull up.

5.4 I^2C Control Interface

PIN	PIN NAME	TYPE	DESCRIPTION
34	SDATA*	I/OD	Serial data of I^2C 2-wire control interface with internal 120KΩ pull-up resistor.
35	SCLK*	IN_{tp120k}	Serial clock of I^2C 2-wire control interface with internal 120KΩ pull-up resistor.

5.5 Power Management Pins

PIN	PIN NAME	TYPE	DESCRIPTION
33	VTT_PWRGD	IN	Power good input signal is power on trapping with HIGH active. This 3.3V input is level sensitive strobe used to determine FS [4:0]. This pin is HIGH active.
	PD#*	IN_{tp120k}	Power Down Function. This is power down pin, low active (PD#). Internal 120K pull up
4	RESET#	OUT	System reset signal when the watchdog is time out. This pin will generate 250ms low phase when the watchdog timer is timeout. Selected by MODE latch input =0.
	CPU_STOP#*	IN_{tp120k}	Active low, Stop all CPU clock outputs. Select by power up latched MODE#=1, internal 120KΩ pull-up resistor.
38	IREF	OUT	Deciding the reference current for the CPU CLOCK pairs. The pin was connected to the precision resistor tied to ground to decide the appropriate current.

5.6 IREF selects Function

BOARD TARGET TRACE/TERM Z	REFERENCE R, IREF = ADD/(3*RR)	OUTPUT CURRENT	VOH @ Z
50 Ω	Rr =221 1% IREF = 5.00mA	Ioh=4*IREF	1.0V @ 50
50 Ω	Rr =475 1% IREF = 2.32mA	Ioh=6*IREF	0.7V @ 50

5.7 Power Pins

PIN	PIN NAME	TYPE	DESCRIPTION
1	VDDREF	PWR	3.3V power supply for REF.
13,19	VDDPCI	PWR	3.3V power supply for PCI.
29	VDDAGP	PWR	3.3V power supply for AGP.
42	VDDCPU	PWR	3.3V power supply for CPU.
28	VDD48	PWR	3.3V power supply for 48MHz.
11	VDDZ	PWR	3.3V power supply for ZCLK.
48	VDDSRC	PWR	3.3V power supply for SRC
36	VDDA	PWR	3.3V power supply for Analog core logic.
5,8,18,23,24,32, 37,41,45	GND	PWR	Ground pin

6. FREQUENCY SELECTION BY HARDWARE OR SOFTWARE

This frequency table is used at power on latched FS [4:0] value or software programming at SSEL [4:0] (Register 0 bit 7 ~ 3).

FS4	FS3	FS2	FS1	FS0	CPU (MHZ)	SRC (MHZ)	ZCLK (MHZ)	AGP (MHZ)	PCI (MHZ)
0	0	0	0	0	100.00	100.00	133.34	66.67	33.33
0	0	0	0	1	100.99	100.00	134.66	67.33	33.66
0	0	0	1	0	102.98	100.00	137.31	68.65	34.33
0	0	0	1	1	100.00	100.00	133.34	66.67	33.33
0	0	1	0	0	133.34	100.00	133.34	66.67	33.33
0	0	1	0	1	134.66	100.00	134.66	67.33	33.66
0	0	1	1	0	137.31	100.00	137.31	68.65	34.33
0	0	1	1	1	133.34	100.00	133.34	66.67	33.33
0	1	0	0	0	200.01	100.00	133.34	66.67	33.33
0	1	0	0	1	201.99	100.00	134.66	67.33	33.66
0	1	0	1	0	205.96	100.00	137.31	68.65	34.33
0	1	0	1	1	200.01	100.00	133.34	66.67	33.33
0	1	1	0	0	166.68	100.00	125.01	62.50	31.25
0	1	1	0	1	168.35	100.00	126.26	63.13	31.57
0	1	1	1	0	171.52	100.00	128.64	64.32	32.16
0	1	1	1	1	166.68	100.00	125.01	62.50	31.25
1	0	0	0	0	105.00	100.00	140.00	70.00	35.00
1	0	0	0	1	106.99	100.00	142.65	71.33	35.66
1	0	0	1	0	109.01	100.00	145.35	72.68	36.34
1	0	0	1	1	109.99	100.00	146.65	73.33	36.66
1	0	1	0	0	140.00	100.00	140.00	70.00	35.00
1	0	1	0	1	142.65	100.00	142.65	71.33	35.66
1	0	1	1	0	145.35	100.00	145.35	72.68	36.34
1	0	1	1	1	146.65	100.00	146.65	73.33	36.66
1	1	0	0	0	210.00	100.00	140.00	70.00	35.00
1	1	0	0	1	213.98	100.00	142.65	71.33	35.66
1	1	0	1	0	218.35	100.00	145.57	72.78	36.39
1	1	0	1	1	219.98	100.00	146.65	73.33	36.66
1	1	1	0	0	266.68	100.00	133.34	66.67	33.33
1	1	1	0	1	269.32	100.00	134.66	67.33	33.66
1	1	1	1	0	274.65	100.00	137.32	68.66	34.33
1	1	1	1	1	266.68	100.00	133.34	66.67	33.33

7. I2C CONTROL AND STATUS REGISTERS

7.1 Register 0: Frequency Select (Default = 20h)

BIT	NAME	PWD	DESCRIPTION
7	SSEL [4]	0	Frequency selection by software via I^2C
6	SSEL [3]	0	
5	SSEL [2]	1	
4	SSEL [1]	0	
3	SSEL [0]	0	
2	EN_SSEL	0	Enable software table selection FS [4:0]. 0 = Hardware table setting (Jump mode). 1 = Software table setting through Bit7~3. (Jump less mode)
1	EN_SPSP	0	Enable spread spectrum mode under clock output. 0 = Spread Spectrum mode disable 1 = Spread Spectrum mode enable
0	EN_SAFE_FREQ	0	After watchdog timeout 0 = Reload the hardware FS [4:0] latched pins setting. 1 = Reload the desirable frequency table selection defined at Reg-5 Bit 4~0.

7.2 Register 1: CPU Control (1 = Enable, 0 = Stopped) (Default: E4h)

BIT	PIN NO	PWD	DESCRIPTION
7	-	1	Reserved
6	44,43	1	CPUT1 / C1 output control
5	40,39	1	CPUT0 / C0 output control
4	15	X	Power on latched value of FS4 pin. Default: 0 (Read only)
3	14	X	Power on latched value of FS3 pin. Default: 0 (Read only)
2	12	X	Power on latched value of FS2 pin. Default: 1 (Read only)
1	3	X	Power on latched value of FS1 pin. Default: 0 (Read only)
0	2	X	Power on latched value of FS0 pin. Default: 0 (Read only)

7.3 Register 2: PCI, ZCLK Control (1 = Enable, 0 = Stopped) (Default: FFh)

BIT	PIN NO	PWD	DESCRIPTION
7	-	1	Reserved
6	15	1	PCI_F1 output control
5	14	1	PCI_F0 output control
4	22	1	ZCLK1 output control
3	21	1	ZCLK0 output control
2	12	1	PCI5 output control
1	22	1	PCI4 output control
0	21	1	PCI3 output control

7.4 Register 3: PCI, AGP Control (1 = Enable, 0 = Stopped) (Default: EFh)

BIT	PIN NO	PWD	DESCRIPTION
7	20	1	PCI2 output control
6	17	1	PCI1 output control
5	16	1	PCI0 output control
4	SEL12_48	X	12 _ 48 MHz output selection, 1: 12 MHz. 0: 48 MHz. (default) Default value follow hardware trapping data on SEL12_48# pin.
3	-	1	Reserved
2	-	1	Reserved
1	30	1	AGP1 output control
0	31	1	AGP0 output control

7.5 Register 4: 48MHz, REF, SRC Control (1 = Enable, 0 = Stopped) (Default: FFh)

BIT	PIN NO	PWD	DESCRIPTION
7	26	1	24_48MHz output control
6	27	1	12_48MHz output control
5	25	1	48MHz output control
4	-	1	Reserved
3	3	1	REF1 output control
2	2	1	REF0 output control
1	47,46	1	SRC output control
0	-	1	Reserved

7.6 Register 5: Watchdog Control (Default: 04h)

BIT	NAME	PWD	DESCRIPTION
7	SEL24_48	X	24 / 48 MHz output selection, 1: 24 MHz, 0: 48 MHz (Default) Default value follow hardware trapping data on SEL24_48# pin.
6	CNT_EN	0	Program this bit => 1: Enable Watchdog Timer feature. 0: Disable Watchdog Timer feature. Read-back this bit => During timer count down the bit read back to 1. If count to zero, this bit read back to 0.
5	WD_TIMEOUT	0	Read Back only. Timeout Flag. This bit is Read Only. 1: Watchdog has ever started and counts to zero. 0: Watchdog is restarted and counting.
4	SAF_FREQ [4]	0	These bits will be reloaded in Reg-0 to select frequency table. As the watchdog is timeout and EN_SAFE_FREQ=1.
3	SAF_FREQ [3]	0	
2	SAF_FREQ [2]	1	
1	SAF_FREQ [1]	0	
0	SAF_FREQ [0]	0	

7.7 Register 6: Skew Control (Default: 25h)

BIT	NAME	PWD	DESCRIPTION
7	Reserved	0	Reserved
6	Reserved	0	Reserved
5	Reserved	1	Reserved
4	Reserved	0	
3	Reserved	0	
2	CSKEW<2>	1	CPU1 to CPU0 skew control Skew resolution is 250ps The decision of skew direction is same as CSKEW<2:0> setting
1	CSKEW<1>	0	
0	CSKEW<0>	1	

7.8 Register 7: Winbond Chip ID (Default: 77h) (Read only)

BIT	NAME	PWD	DESCRIPTION
7	CHPI_ID [7]	0	Winbond Chip ID. W83194BR-655 (SA5877).
6	CHPI_ID [6]	1	Winbond Chip ID.
5	CHPI_ID [5]	1	Winbond Chip ID.
4	CHPI_ID [4]	1	Winbond Chip ID.
3	CHPI_ID [3]	0	Winbond Chip ID.
2	CHPI_ID [2]	1	Winbond Chip ID.
1	CHPI_ID [1]	1	Winbond Chip ID.
0	CHPI_ID [0]	1	Winbond Chip ID.

7.9 Register 8: M/N (Default: 90h)

BIT	NAME	PWD	DESCRIPTION
7	NVAL<8>	X	Programmable N divisor value. Bit 7 ~0 are defined in the Register 9.
6	MVAL<6>	X	Programmable M divisor
5	MVAL<5>	X	
4	MVAL<4>	X	
3	MVAL<3>	X	
2	MVAL<2>	X	
1	MVAL<1>	X	
0	MVAL<0>	X	

7.10 Register 9: N (Default: BBh)

BIT	NAME	PWD	DESCRIPTION
7	NVAL<7>	X	Programmable N divisor bit 7 ~0. The bit 8 is defined in Register 8, The bit 9 is defined in Register 10
6	NVAL<6>	X	
5	NVAL<5>	X	
4	NVAL<4>	X	
3	NVAL<3>	X	
2	NVAL<2>	X	
1	NVAL<1>	X	
0	NVAL<0>	X	

7.11 Register 10:N & N3 (Default: 3Bh)

BIT	NAME	PWD	DESCRIPTION
7	NVAL<9>	X	Programmable N divisor bit 9.
6	N3VAL<6>	X	Programmable N3 divisor bit 6 ~0 for programmable
5	N3VAL<5>	X	SRC clock.
4	N3VAL<4>	X	PS: Frequency range: 86.8M ~ 115.2M
3	N3VAL<3>	X	Resolution: 224K
2	N3VAL<2>	X	
1	N3VAL<1>	X	
0	N3VAL<0>	X	

7.12 Register 11: Spread Spectrum Programming (Default: 0Eh)

BIT	NAME	PWD	DESCRIPTION
7	SP_UP [3]	0	Spread Spectrum Up Counter bit 3 ~ bit 0.
6	SP_UP [2]	0	
5	SP_UP [1]	0	
4	SP_UP [0]	0	
3	SP_DOWN [3]	1	Spread Spectrum Down Counter bit 3 ~ bit 0
2	SP_DOWN [2]	1	2's complement representation.
1	SP_DOWN [1]	1	Ex: 1 -> 1111; 2 -> 1110; 7 -> 1001; 8 -> 1000
0	SP_DOWN [0]	0	

7.13 Register 12: Divisor and Step-less Enable Control (Default: 89h)

BIT	NAME	PWD	DESCRIPTION
7	M_NACC_EN	1	Enable variable accumulation period for M divisor 1: Enable, 0: Disable (Original timing)
6	KVAL<9>	X	Define the ZCLK divider ratio
5	KVAL<5>	X	Table-2 integrate the all divider configuration
4	Reserved	X	Reserved
3	Reserved	X	
2	KVAL<2>	X	Define the CPU divider ratio
1	KVAL<1>	X	Refer to Table-2
0	KVAL<0>	X	

Table-2 CPU, ZCLK, divider ratio selection Table

LSB / MSB		ZCLK		CPU			
		BIT5		BIT1, 0			
		0	1	00	01	10	11
Bit2/ Bit4/ Bit9	0	Div3	Div4	Div2	Div3	Div4	Div5
	1	Div5	Div6	Div6	Div8	Div8	Div8

7.14 Register 13: M/N Control (Default: 0Ah)

BIT	NAME	PWD	DESCRIPTION
7	EN_MN_PROG	0	0: Output frequency depend on frequency table 1: Program all clock frequency by changing M/N value The equation is **VCO =14.318MHz*(N+4)/ M**. Once the watchdog timer timeout, the bit will be clear. Then the frequency will be decided by hardware default FS<4:0> or desired frequency select SAF_FREQ [4:0] depend on EN_SAFE_FREQ (Reg0 - bit 7).
6	NVAL<10>	X	Programmable N divisor bit 10.
5	DIVM_P1	0	Variable accumulation period for M divisor. Depend
4	DIVM_P0	0	On VCO Frequency. 00: 400M 01: 533M 10: 667M 11: 800M
3	IVAL<3>	X	Charge pump current selection
2	IVAL<2>	X	
1	IVAL<1>	X	
0	IVAL<0>	X	

7.15 Register 14: Reserved (Default: 10h)

BIT	NAME	PWD	DESCRIPTION
7	CPUT_DRI	0	CPUT output state in during POWER DOWN or Stop mode assertion. 1: Driven (2*Iref) 0: Tristate (Floating) CPUC always tri-state (floating) in power down Assertion.
6	SRCT_DRI	0	SRC_T output state in during POWER DOWN or Stop mode assertion. 1: Driven (6*Iref => STOP mode) (2*Iref => POWER DOWN) 0: Tristate (Floating) SRC_C always tri-state (floating) in power down Assertion.
5	SPCNT<5>	0	Spread Spectrum Programmable time, the resolution is 280ns. Default period is 11.8us
4	SPCNT<4>	1	
3	SPCNT<3>	0	
2	SPCNT<2>	0	
1	SPCNT<1>	0	
0	SPCNT<0>	0	

7.16 Register 15: Spread Spectrum type Control (Default: 2Ch)

BIT	NAME	PWD	DESCRIPTION
7	INV_CPU	0	Invert the CPU phase, 0: Default, 1: Inverse
6	INV_ZCLK	0	Invert the ZCLK phase, 0: Default, 1: Inverse
5	SPSP_TYPE	1	Spread spectrum implementation method 1: Pendulum type, 0: Original
4	SPSP1	0	Spread Spectrum type select. 00: Down 1% 01: Down 0.5% 10: Center +/- 0.5% 11: Center +/- 0.25%
3	SPSP0	1	
2	ASKEW<2>	1	CPU1 to AGP skew control. Skew resolution is 250ps The decision of skew direction is same as ASKEW<2:0> setting
1	ASKEW<1>	0	
0	ASKEW<0>	0	

7.17 Register 16: Skew Control (Default: 24h)

BIT	NAME	PWD	DESCRIPTION
7	INV_AGP	0	Invert the AGP phase, 0: Default, 1: Inverse
6	INV_PCI	0	Invert the PCI phase, 0: Default, 1: Inverse
5	ZSKEW<2>	1	CPU1 to ZCLK skew control
4	ZSKEW<1>	0	Skew resolution is 250ps
3	ZSKEW<0>	0	The decision of skew direction is same as ZSKEW<2:0> setting
2	PSKEW<2>	1	CPU1 to PCI skew control
1	PSKEW<1>	0	Skew resolution is 250ps
0	PSKEW<0>	0	The decision of skew direction is same as PSKEW<2:0> setting

7.18 Register 17: Slew rate Control (Default: 00h)

BIT	NAME	PWD	DESCRIPTION
7	INV_SRC	0	Invert the SRC phase, 0: Default, 1: Inverse.
6	INV_USB12	0	Invert the USB12_48 phase, 0: In phase with USB24_48 1: 180 degrees out of phase
5	PCI_F0_S2	0	PCI_F1 / PCI_F0 slew rate control
4	PCI_F0_S1	0	11: Strong, 00: Weak, 10/01: Normal
3	Reserved	0	Reserved
2	Reserved	0	
1	AGP_10_S2	0	AGP_1 / AGP_0 slew rate control
0	AGP_10_S1	0	11: Strong, 00: Weak, 10/01: Normal

7.19 Register 18: Slew rate Control (Default: 00h)

BIT	NAME	PWD	DESCRIPTION
7	PCI_5_S2	0	PCI5 slew rate control
6	PCI_5_S1	0	11: Strong, 00: Weak, 10/01: Normal
5	PCI_42_S2	0	PCI4, 3,2 slew rate control
4	PCI_42_S1	0	11: Strong, 00: Weak, 10/01: Normal
3	PCI_10_S2	0	PCI1, 0 slew rate control
2	PCI_10_S1	0	11: Strong, 00: Weak, 10/01: Normal
1	REF_S2	0	REF0, 1 slew rate control
0	REF_S1	0	11: Strong, 00: Weak, 10/01: Normal

7.20 Register 19: Slew rate Control (Default: D2h)

BIT	NAME	PWD	DESCRIPTION
7	CPU1S_EN	1	Stop CPU1 clocks, 1: Enable stop feature, 0: Disable
6	CPU0S_EN	1	Stop CPU0 clocks, 1: Enable stop feature, 0: Disable
5	ZCLK_S2	0	ZCLK1, 0 slew rate control
4	ZCLK_S1	1	11: Strong, 00: Weak, 10/01: Normal
3	INV_USB48	0	Invert the USB48 phase, 0: In phase with USB24_48 1: 180 degrees out of phase
2	USB48_S2	0	USB48/USB12_48/USB24_48 slew rate control
1	USB48_S1	1	11: Strong, 00: Weak, 10/01: Normal
0	MODE	X	Desktop / Mobile Mode (pin 4,pin16) selection, 1: Mobile mode (CPUSTOP#, PCISTOP), 0: Desktop mode (Default)(RESET#,PCI0), Default value follow hardware trapping data on MODE pin.

7.21 Register 20: Watch dog timer (Default: 88h)

BIT	NAME	PWD	DESCRIPTION
7	Reserved	1	Reserved for test use, don't modify it.
6	SEC<6>	0	Setting the down count depth. One bit resolution Represent 250ms. Default time depth is 8*250ms = 2.0 second. If the watchdog timer is counting, this register will return present down count value.
5	SEC<5>	0	
4	SEC<4>	0	
3	SEC<3>	1	
2	SEC<2>	0	
1	SEC<1>	0	
0	SEC<0>	0	

7.22 Register 21: Fix Control (Default: 00h)

BIT	NAME	PWD	DESCRIPTION
7	TRI-EN	0	Tri-state all output if set 1
6	FIX_ZCLK	0	ZCLK output frequency select mode (Only valid under FIX_ADDR<2:0> is nonzero) 0: Output frequency according to frequency selection table 1: Output frequency according to FIX frequency table
5	FIX_PCI	0	PCI output frequency select mode (Only valid under FIX_ADDR<2:0> is nonzero) 0: Output frequency according to frequency selection table 1: Output frequency according to FIX frequency table

Register 21: Fix Control (Default: 00h), continued

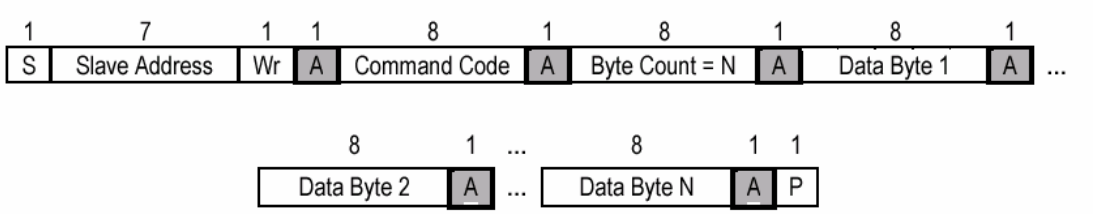
BIT	NAME	PWD	DESCRIPTION
4	FIX_AGP	0	AGP output frequency select mode (Only valid under FIX_ADDR<2:0> is nonzero) 0: Output frequency according to frequency selection table 1: Output frequency according to FIX frequency table
3	Reserved	0	Reserved for test use, don't modify it.
2	FIX_ADDR<2>	0	Asynchronous ZCLK/AGP/PCI frequency table selection
1	FIX_ADDR<1>	0	FIX_ADDR<2:0>
0	FIX_ADDR<0>	0	001: 132 / 66 / 33M 010:132 / 75.43 / 37.7M 011: 132 / 88 / 44M 100:176 / 88 / 44M 101: 132 / 66 / 33M 110:132 / 75.43 / 33M 111: 132 / 88 / 33M 000: Clock from PLL1

8. ACCESS INTERFACE

The W83194BR-655 provides I²C Serial Bus for microprocessor to read/write internal registers. In the W83194BR-655 is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I²C address is defined at 0xD2.

Block Read and Block Write Protocol

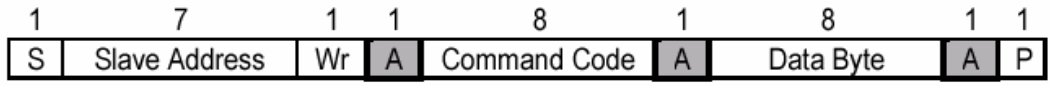
8.1 Block Write protocol



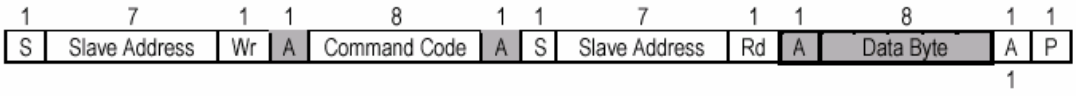
8.2 Block Read protocol

In block mode, the command code must filled 8'h00

8.3 Byte Write protocol



8.4 Byte Read protocol



9. SPECIFICATIONS

9.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or VDD).

PARAMETER	RATING
Absolute 3.3V Core Supply Voltage	-0.5V to +4.6V
Absolute 3.3V I/O Supple Voltage	- 0.5 V to + 4.6 V
Operating 3.3V Core Supply Voltage	3.135V to 3.465V
Operating 3.3V I/O Supple Voltage	3.135V to 3.465V
Storage Temperature	- 65°C to + 150°C
Ambient Temperature	- 55°C to + 125°C
Operating Temperature	0°C to + 70°C
Input ESD protection (Human body model)	2000V

9.2 General Operating Characteristics

VDD48=VDDAGP=VDDREF=VDDPCI= 3.3V ± 5 %, TA = 0℃ to +70℃, CI=10pF					
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Input Low Voltage	V_{IL}		0.8	V_{dc}	
Input High Voltage	V_{IH}	2.0		V_{dc}	
Output Low Voltage	V_{OL}		0.4	V_{dc}	All outputs using 3.3V power
Output High Voltage	V_{OH}	2.4		V_{dc}	All outputs using 3.3V power
Operating Supply Current	I_{dd}		350	mA	CPU = 100 to 200 MHz PCI = 33.3 Mhz with load
Input pin capacitance	Cin		5	pF	
Output pin capacitance	Cout		6	pF	
Input pin inductance	Lin		7	nH	

9.3 Skew Group timing clock

VDD48=VDDAGP=VDDREF=VDDPCI = 3.3V ± 5 %, TA = 0℃ to +70℃, CI=10pF					
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**	**TEST CONDITIONS**
AGP to PCI Skew	1.5	2.6	3.5	ns	Measured at 1.5V
CPU to CPU Skew			150	ps	Crossing point
AGP to AGP Skew			175	ps	Measured at 1.5V
PCI to PCI Skew			500	ps	Measured at 1.5V
48MHz to 48MHz Skew			1000	ps	Measured at 1.5V
REF to REF Skew			500	ps	Measured at 1.5V

9.4 CPU 0.7V Electrical Characteristics

VDDCPU= 3.3V ± 5 %, TA = 0℃ to +70℃,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	175	700	ps	100 to 200 Mhz, Measure from Vol=0.175 to Voh=0.525
Fall Time	175	700	ps	100 to 200Mhz, Measure from Vol=0.175 to Voh=0.525
Absolute crossing point Voltages	250	550	mV	100 to 200Mhz,
Cycle to Cycle jitter		125	ps	100 to 200Mhz, Measure from differential wavefrom
Duty Cycle	45	55	%	100 to 200Mhz, Measure from differential wavefrom

9.5 SRC 0.7V Electrical Characteristics

VDDSRC= 3.3V ± 5 %, TA = 0℃ to +70℃,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	175	700	ps	100 Mhz , Measure from Vol=0.175 to Voh=0.525
Fall Time	175	700	ps	100 Mhz, Measure from Vol=0.175 to Voh=0.525
Absolute crossing point Voltages	250	550	mV	100 Mhz
Cycle to Cycle jitter		125	ps	100 Mhz, Measure from differential wavefrom
Duty Cycle	45	55	%	100 Mhz, Measure from differential wavefrom

9.6 AGP Electrical Characteristics

VDDAGP= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	500	2000	ps	Measure from 0.4V to 2.4V
Fall Time	500	2000	ps	Measure from 2.4V to 0.4V
Cycle to Cycle jitter		250	ps	Measure 1.5V point
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.7 PCI Electrical Characteristics

VDDPCI= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	500	2000	ps	Measure from 0.4V to 2.4V
Fall Time	500	2000	ps	Measure from 2.4V to 0.4V
Cycle to Cycle jitter		250	ps	Measure 1.5V point
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.8 12, 24M, 48M Electrical Characteristics

VDD48= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	1000	2000	ps	Measure from 0.4V to 2.4V
Fall Time	1000	2000	ps	Measure from 2.4V to 0.4V
Long term jitter		2000	ps	Measure 1.5V point
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

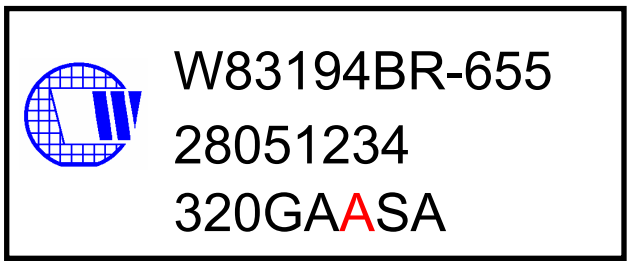
9.9 REF Electrical Characteristics

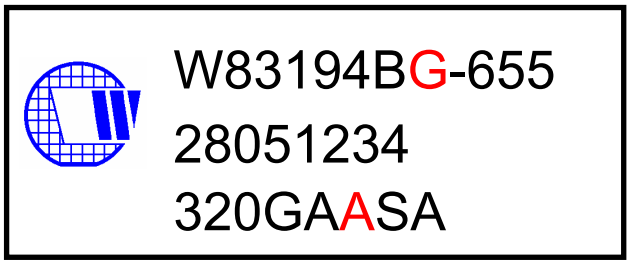
VDDREF= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	1000	4000	ps	Measure from 0.4V to 2.4V
Fall Time	1000	4000	ps	Measure from 2.4V to 0.4V
Cycle to Cycle jitter		1000	ps	Measure 1.5V point
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

10. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83194BR-655	48 PIN SSOP	Commercial, 0°C to +70°C
W83194BG-655	48 PIN SSOP (Pb free part)	Commercial, 0°C to +70°C

11. HOW TO READ THE TOP MARKING





1st line: Winbond logo and the type number: W83194BR-655

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 320 G A A SA

320: packages made in '2003, week 20

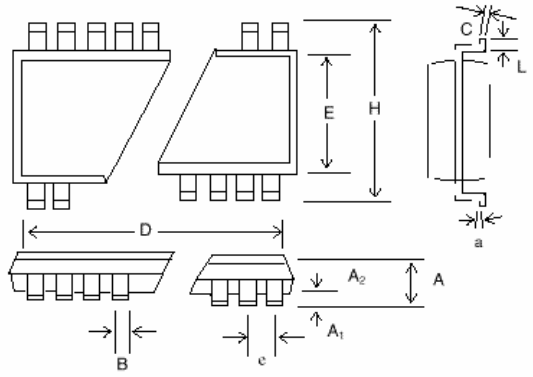
G: assembly house ID; O means OSE, G means GR

A: Internal use code

A: IC revision

SA: Internal use code

12. PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

Important Notice

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