Features

- Microprocessor Interface
  - – I^2C bus interface
  - – Supports various microprocessors
    LSI, 68xxx, ST20, PowerPC, Conexant, etc.
  - – PC card control signals generation
    Memory and Attribute memory mode
- MPEG Video Stream Interface
  - – MPEG II Transport Stream compliant
- Common Interface Module Interface
  - – Common interface standard compliant
  - – PC Card Standard compliant
  - – Hot Insertion capability
  - – Polling and Interrupt modes
  - – Two full independent module capability
- 3.3V for all outputs, 5.0V tolerant for all inputs
- MQFP 128 pin Package

General Description

StarCI is the common interface controller for digital satellite video receiver and digital TV to adopt the common interface standard(CENELEC EN-50221).

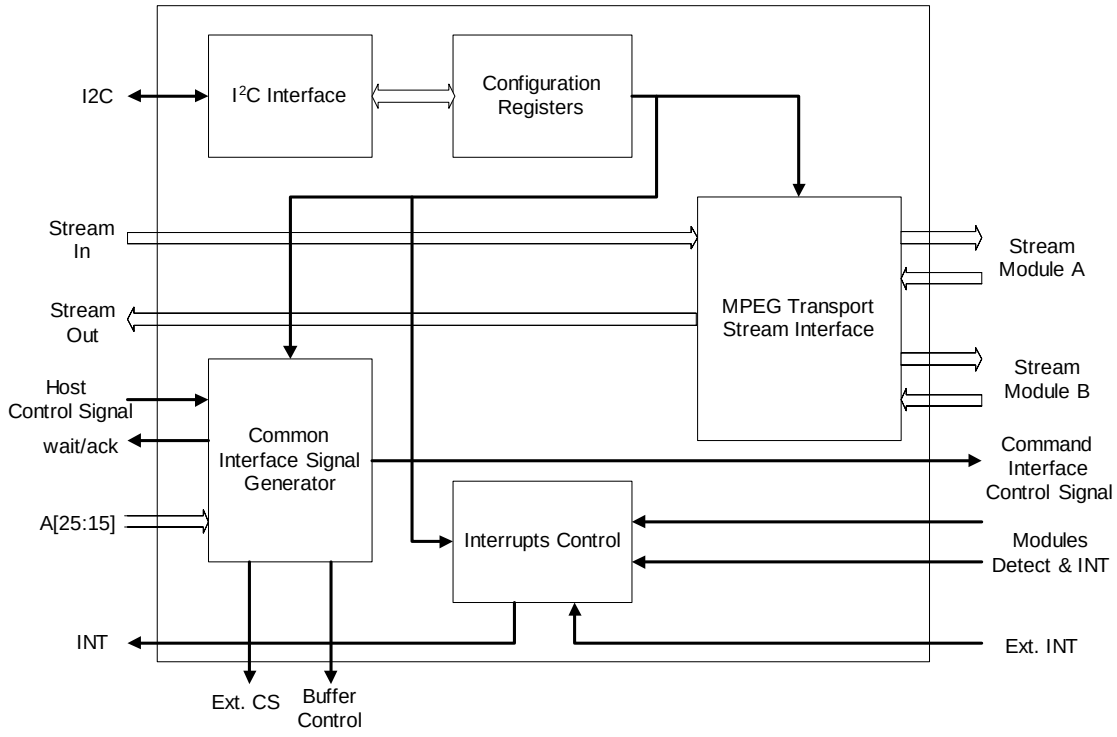
Through *StarCI*, the receiver's microprocessor reads the status of the common interface modules and gives a command to the modules and then the modules processes the MPEG video stream.

After *StarCI* is initialized by I^2C bus connected with the microprocessor, it generates the command interface control signals to agree the specification of each module from the control signals of the microprocessor. *StarCI* supports the interface of various microprocessors for flexible implementation of the receiver.

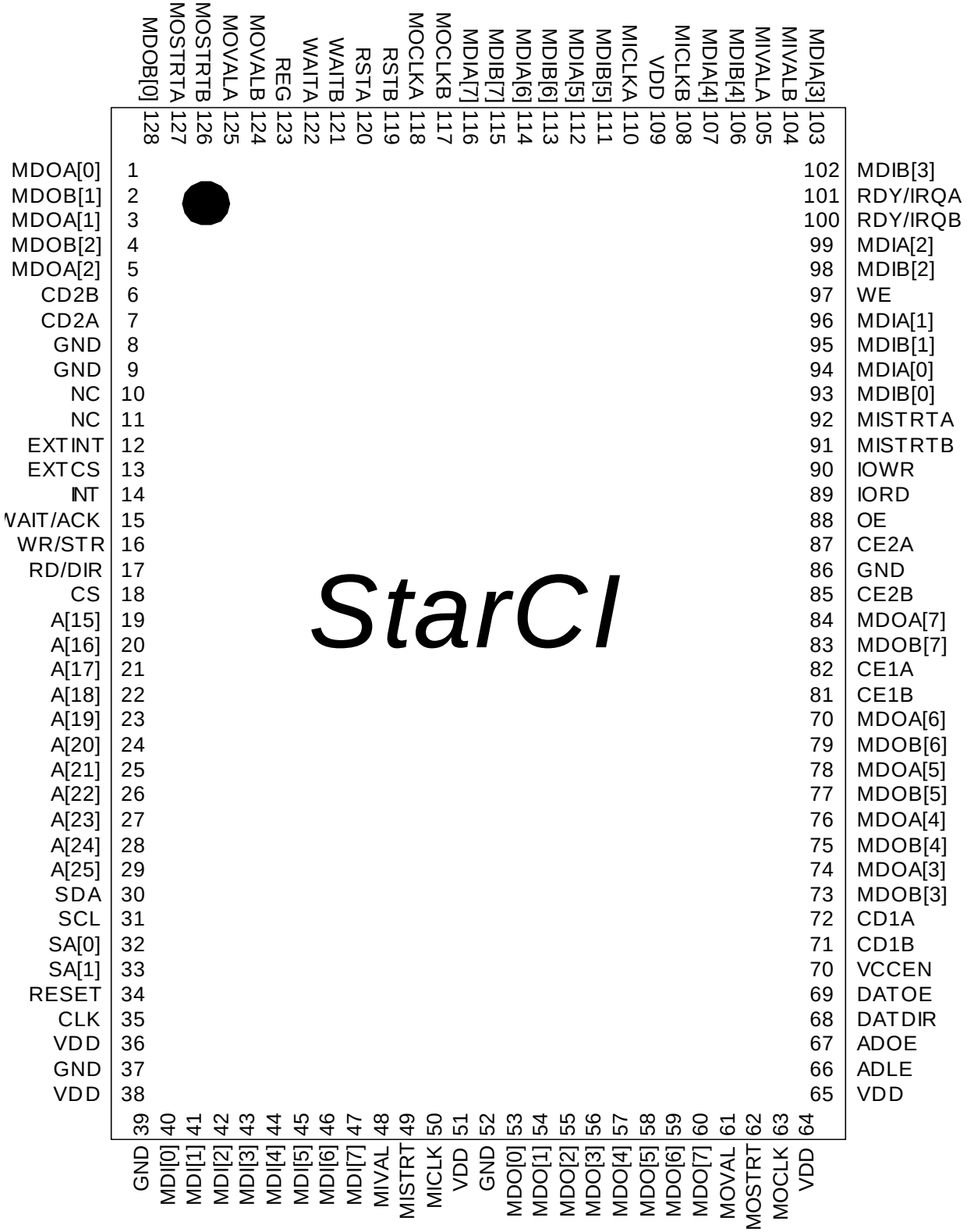
StarCI is able to simultaneously control two independent modules and to support hot-insertion of them.

In addition, instead of the common interface modules, *StarCI* supports to use 8-bit memory card to be based on PC Card Standard, which is capable of memory extension of receiver.

Block Diagram



Package



MQFP 128 pin configuration

Pin Descriptions

Pin Number	Name	I/O	Type	Description
1	MDOA[0]	I	CMOS down	MPEG data input from module A
2	MDOB[1]	I	CMOS down	MPEG data input from module B
3	MDOA[1]	I	CMOS down	MPEG data input from module A
4	MDOB[2]	I	CMOS down	MPEG data input from module B
5	MDOA[2]	I	CMOS down	MPEG data input from module A
6	CD2B	I	CMOS up	Card detect signal 2 of module B
7	CD2A	I	CMOS up	Card detect signal 2 of module A
8	GND		Power	
9	GND		Power	
10	N.C.			
11	N.C.			
12	EXTINT	I	CMOS	Interrupt signal of external device
13	EXTCS	O	CMOS TS	Chip select signal of external device
14	INT	O	CMOS TS	Interrupt output to microprocessor
15	WAIT/ACK	O	CMOS TS	Wait or acknowledge signal to microprocessor
16	WR/STR	I	CMOS	Write or strobe signal from microprocessor
17	RD/DIR	I	CMOS	Read or direction signal from microprocessor
18	CS	I	CMOS	Chip select signal from microprocessor
19	A[15]	I	CMOS	Address output bit 15of microprocessor
20	A[16]	I	CMOS	Address output bit 16 of microprocessor
21	A[17]	I	CMOS	Address output bit 17 of microprocessor
22	A[18]	I	CMOS	Address output bit 18 of microprocessor
23	A[19]	I	CMOS	Address output bit 19 of microprocessor
24	A[20]	I	CMOS	Address output bit 20 of microprocessor
25	A[21]	I	CMOS	Address output bit 21 of microprocessor
26	A[22]	I	CMOS	Address output bit 22 of microprocessor
27	A[23]	I	CMOS	Address output bit 23 of microprocessor
28	A[24]	I	CMOS	Address output bit 24 of microprocessor
29	A[25]	I	CMOS	Address output bit 25 of microprocessor
30	SDA	I/O	TTL	I^2C data
31	SCL	I	TTL	I^2C clock
32	SA[0]	I	CMOS	I^2C address bit 0
33	SA[1]	I	CMOS	I^2C address bit 1
34	RESET	I	CMOS	Chip reset – high active
35	CLK	I	CMOS	Clock input – 27 MHz
36	VDD		Power	
37	GND		Power	
38	VDD		Power	
39	GND		Power	
40	MDI[0]	I	CMOS	MPEG data input
41	MDI[1]	I	CMOS	MPEG data input
42	MDI[2]	I	CMOS	MPEG data input
43	MDI[3]	I	CMOS	MPEG data input

Pin Number	Name	I/O	Type	Description
44	MDI[4]	I	CMOS	MPEG data input
45	MDI[5]	I	CMOS	MPEG data input
46	MDI[6]	I	CMOS	MPEG data input
47	MDI[7]	I	CMOS	MPEG data input
48	MIVAL	I	CMOS	MPEG data valid signal input
49	MISTRT	I	CMOS	MPEG data start signal input
50	MICLK	I	CMOS	MPEG clock signal input
51	VDD		Power	
52	GND		Power	
53	MDO[0]	O	CMOS	MPEG data output
54	MDO[1]	O	CMOS	MPEG data output
55	MDO[2]	O	CMOS	MPEG data output
56	MDO[3]	O	CMOS	MPEG data output
57	MDO[4]	O	CMOS	MPEG data output
58	MDO[5]	O	CMOS	MPEG data output
59	MDO[6]	O	CMOS	MPEG data output
60	MDO[7]	O	CMOS	MPEG data output
61	MOVAL	O	CMOS	MPEG data valid signal output
62	MOSTRT	O	CMOS	MPEG data start signal output
63	MOCLK	O	CMOS	MPEG clock signal output
64	VDD		Power	
65	VDD		Power	
66	ADLE	O	CMOS	External address buffer latch enable signal
67	ADOE	O	CMOS	External address buffer output enable signal
68	DATDIR	O	CMOS	External data buffer direction
69	DATOE	O	CMOS	External data buffer output enable
70	VCCEN	O	CMOS TS	VCC switch control signal of modules
71	CD1B	I	CMOS up	Card detect signal 1 of module B
72	CD1A	I	CMOS up	Card detect signal 1 of module A
73	MDOB[3]	I	CMOS down	MPEG data input from module B
74	MDOA[3]	I	CMOS down	MPEG data input from module A
75	MDOB[4]	I	CMOS down	MPEG data input from module B
76	MDOA[4]	I	CMOS down	MPEG data input from module A
77	MDOB[5]	I	CMOS down	MPEG data input from module B
78	MDOA[5]	I	CMOS down	MPEG data input from module A
79	MDOB[6]	I	CMOS down	MPEG data input from module B
80	MDOA[6]	I	CMOS down	MPEG data input from module A
81	CE1B	O	CMOS TS	Card enable signal 1 of module B
82	CE1A	O	CMOS TS	Card enable signal 1 of module A
83	MDOB[7]	I	TTL down	MPEG data input from module B
84	MDOA[7]	I	TTL down	MPEG data input from module A
85	CE2B	O	CMOS TS	Card enable signal 2 of module B
86	GND		Power	
87	CE2A	O	CMOS TS	Card enable signal 2 of module A

Pin Number	Name	I/O	Type	Description
88	OE	O	CMOS TS	Output enable signal to modules
89	IORD	O	CMOS TS	I/O read signal tomodules
90	IOWR	O	CMOS TS	I/O write signal to modules
91	MISTRTB	O	CMOS TS	MPEG data start signal to module B
92	MISTRTA	O	CMOS TS	MPEG data start signal to module A
93	MDIB[0]	O	CMOS TS	MPEG data output to module B
94	MDIA[0]	O	CMOS TS	MPEG data output to module A
95	MDIB[1]	O	CMOS TS	MPEG data output to module B
96	MDIA[1]	O	CMOS TS	MPEG data output to module A
97	WE	O	CMOS TS	Write enable signal to modules
98	MDIB[2]	O	CMOS TS	MPEG data output to module B
99	MDIA[2]	O	CMOS TS	MPEG data output to module A
100	RDY/IRQB	I	CMOS	RDY/IRQ signal from module B
101	RDY/IRQA	I	CMOS	RDY/IRQ signal from module A
102	MDIB[3]	O	CMOS TS	MPEG data output to module B
103	MDIA[3]	O	CMOS TS	MPEG data output to module A
104	MIVALB	O	CMOS TS	MPEG data valid signal to module B
105	MIVALA	O	CMOS TS	MPEG data valid signal to module A
106	MDIB[4]	O	CMOS TS	MPEG data output to module B
107	MDIA[4]	O	CMOS TS	MPEG data output to module A
108	MICLKB	O	CMOS TS	MPEG clock signal to module B
109	VDD		Power	
110	MICLKA	O	CMOS TS	MPEG clock signal to module A
111	MDIB[5]	O	CMOS TS	MPEG data output to module B
112	MDIA[5]	O	CMOS TS	MPEG data output to module A
113	MDIB[6]	O	CMOS TS	MPEG data output to module B
114	MDIA[6]	O	CMOS TS	MPEG data output to module A
115	MDIB[7]	O	CMOS TS	MPEG data output to module B
116	MDIA[7]	O	CMOS TS	MPEG data output to module A
117	MOCLKB	I	CMOS down	MPEG clock signal from module B
118	MOCLKA	I	CMOS down	MPEG clock signal from module A
119	RSTB	O	CMOS TS	Reset of module B
120	RSTA	O	CMOS TS	Reset of module A
121	WAITB	I	CMOS	WAIT signal of module B
122	WAITA	I	CMOS	WAIT signal of module A
123	REG	O	CMOS TS	REG signal to modules
124	MOVALB	I	CMOS down	MPEG data valid input from module B
125	MOVALA	I	CMOS down	MPEG data valid input from module A
126	MOSTRTB	I	CMOS down	MPEG data start input from module B
127	MOSTRTA	I	CMOS down	MPEG data start input from module A
128	MDOB[0]	I	CMOS down	MPEG data input to module B

Notations : TTL(TTL level), CMOS(CMOS level), TS(Tristate), up(internal pull-up), down(internal pull-down)

Function Descriptions

Microprocessor interface

StarCI uses a clock oscillator of 27MHz frequency with a duty cycle between 33% and 67%.

StarCI is initialized by setting the 26 registers through a I^2C interface. The I^2C device address can be chosen among four values by connecting SA1 and SA0 to VCC or GND. The base address can be chosen between 80h, 82h, 84h or 86h allowing the connection of up to four StarCI on the same bus.

Refer to I^2C standard of Philips data book for the detailed AC/DC characteristics and the timing diagram of the I^2C interface .

StarCI supports a bus control of various microprocessors. At reset, the host microprocessor interface is disabled – CS, RD/DIR and WR/STR inputs are inactive and WAIT/ACK and INT are in high impedance state. The only available access is the configuration interface(I^2C) which permits to set up the StarCI.

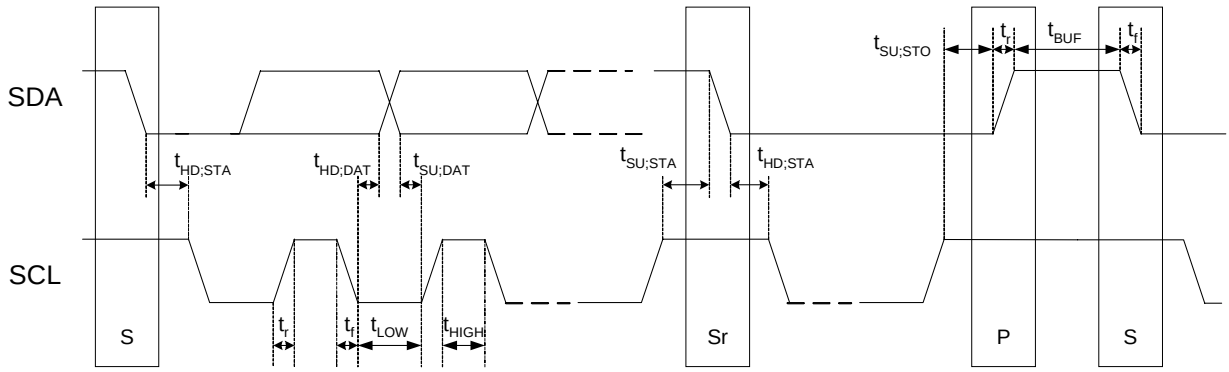
Once the proper parameters have been entered in the StarCI, the interface is enabled by setting the LOCK bit in the control register('h1F). The access to the modules is then possible and some parameters related to the host microprocessor interface are impossible to modify.

Host microprocessor input control signals are CS, RD/DIR, WR/STR and output signals are WAIT/ACK and INT. Input and output active levels can be individually set up by configuration bits. The output buffer structure is also configurable to be either open-drain or push-pull.

StarCI inputs the RD/DIR, WR/STR and CS signals from host microprocessor, WAITA and WAITB from the modules and generates all the control signals to modules, host microprocessor, buffers and external device : CE1A, CE2A, CE1B, CE2B, REG, OE, WE, IORD, IOWR, WAIT, ACK, ADLE, DATDIR, DATOE.

I^2C interface

The I^2C bus timing characteristics, and bus-line capacitance are given in below table, and below figure shows the timing definitions for the I^2C bus. The minimum HIGH and LOW periods of the SCL clock specified in below table determine the maximum bit transfer rates of 400 kbits/sec for Fast-mode.



Definition of timing for Fast-mode on the I^2C bus

Characteristics of the SDA and SCL bus lines for Fast-mode

Parameter	Symbol	Min	Max	Unit
SCL clock frequency	f_{scl}		400	KHz
Bus free time between stop and start	t_{BUF}	1.3		µsec
Hold time start condition	$t_{HD,STA}$	0.3		µsec
SCL low period	t_{LOW}	1.3		µsec
SCL high period	t_{HIGH}	0.6		µsec
Setup time before a repeated start	$t_{SU,STA}$	0.6		µsec
Data hold time	$t_{HD,DAT}$	0	0.9	µsec
Data setup time	$t_{SU,DAT}$	100		nsec
Rise time for both SDA and SCL signals	t_r	20	300	nsec
Fall time for both SDA and SCL signals	t_f	20	300	nsec
Setup time before a stop condition	$t_{SU,STO}$	0.6		µsec
Capacitive load for each bus line	C_b		400	PF

Microprocessor control signals

Host microprocessor input control signals are CS, RD/DIR, WR/STR and output signals are WAIT/ACK and INT. Input and output active levels can be individually set up by configuration bits, and the output buffer structure is also configurable to be either open-drain or push-pull in the UCSG1 and UCSG2 registers.

The INT output to the microprocessor can be configured to be active high or low and driven by a push-pull or open-drain. Interrupts are managed by StarCI and one output is available for connection StarCI to the microprocessor interrupt controller. Five interrupt sources are available: two modules detection, two modules IRQ, and one external device interrupt. Modules detection interrupts are latched inside the StarCI and are acknowledged on the reading of the Interrupt Status Register. Each interrupt source can be individually masked. When masked, an incoming interrupt is visible in the Interrupt Status Register but does not generate an interrupt to the host microprocessor.

Command interface

The command interface is directly issued from PC Card standard restricted to 8 bits access and 15 bits addressing. The command interface of a CI module is described in detail in the PC Card standard and the restrictions applied to this standard for the command interface are described in the DVB CI standard. The 15 address bits and 8 data bits of the CI modules are connected to the host microprocessor bus through tri-state buffers (type 373 and 245) which are controlled by the StarCI which outputs an output enable and a direction control signal for each buffer group.

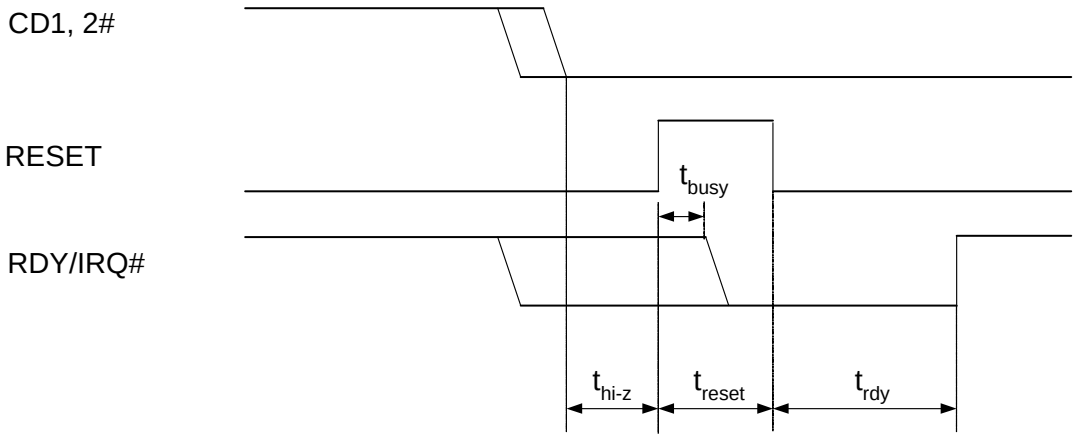
StarCI provides the buffers control signals. The buffers should be powered by the same source as the modules.

The CI control signals are the same as the PC Card control signal : CE1, CE2, REG, OE, WE, IORD, IOWR, RDY/IRQ, WAIT. StarCI generates those signals so that they fit the PC Card standard whenever the host microprocessor accesses one of the modules.

The control signals activated depend on the access type chosen in the module control register with ACS[1:0]. The read and write signals active level duration is configured in the memory access cycle time registers. StarCI receives RDY/IRQ from the module and retransmits the interruption to the host microprocessor. The module can also send a WAIT request that is also transmitted to the host microprocessor in addition to the wait states already generated due to the read and write duration.

Module Detection and Activation

The StarCI automatically detects the insertion and removal of a module and acts as programmed whenever this occurs. In order to detect a module, two pins on the connector: CD1# and CD2# must be simultaneously asserted to ensure a module is inserted. When a module is inserted, the StarCI can automatically activate the module if programmed so when AUTO bit is asserted in the Module Control Register. The activation can also be handled manually by the host microprocessor by asserting the bits in the Module Control Register. The module activation consists in resetting the module and waiting for RDY signal to go high with respect to the PC card standard timings.

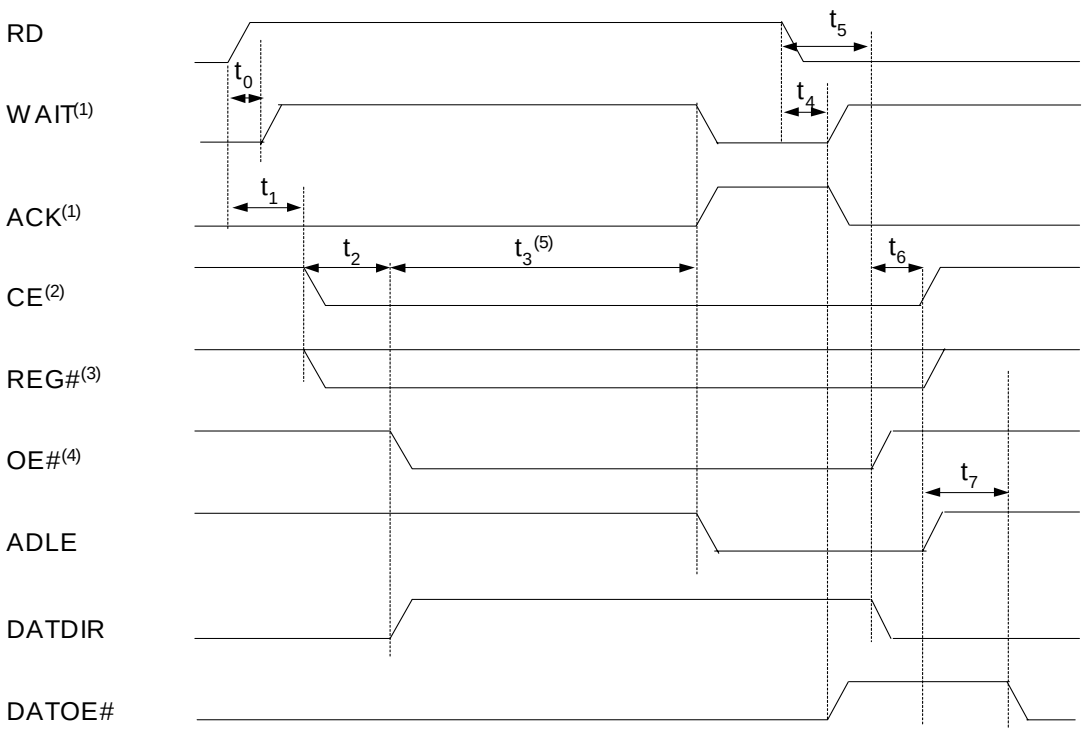


Procedure of the module detection

Parameter	Symbol	Min	Max	Unit
Card detect to reset driven	t_{hi-z}	329		msec
Reset pulse width	t_{reset}	11		µsec
Reset asserted to ready negated	t_{busy}		10	µsec
Reset negated to module ready	t_{rdy}		5	sec

Module Read Access

Memory read timings are given for various cycle duration. In attribute memory mode, only 600 nsec and 300 nsec cycles are available. In common memory mode, 300 nsec doesn't exist. IO and external device in regenerate mode share the same timing specifications as they all use IORD# and IOWR# signals. Timings are given in StarCI clock cycles. They are calculated to comply with PCMCIA specifications when 27 MHz clock is used.



Notes

(1) The WAIT/ACK output is either WAIT or ACK formatted according to the WAIT/ACK pin settings (driving structure, active level)

(2) Depending on the read access type, CE can be either CE1A# or CE1B# for access to memory or IO mode to module A or B, CE2A# or CE2B# for access in EC(Extended Channel) mode, or even EXTCS for access to external device in regenerate mode.

(3) REG# signal is not asserted during a common memory or external access.

(4) OE# signal is asserted during a memory access(attribute or common). It is replaced by IORD# during an IO read cycle, an EC read cycle, or an external device in regenerate mode.

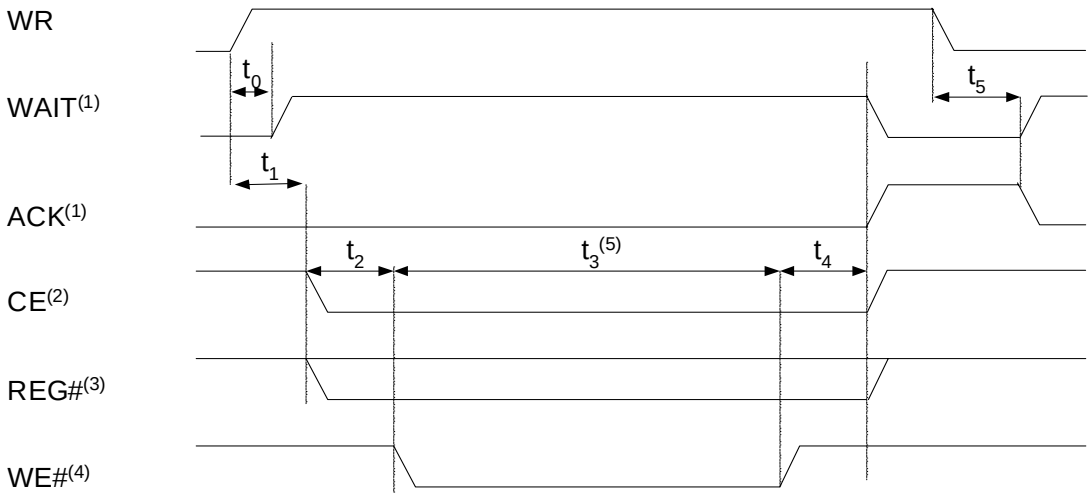
(5) t2 can be lengthened by the insertion of wait cycles. When the module asserts WAIT# signal, t2 cycles counter stops until WAIT# becomes inactive anew

*unit : ns(cycle)

	Memory read						IO,EC, EXT
	600	300	250	200	150	100	
t0 max	15						
t1 max	74(2)						
t2	111(3)	37(1)	37(1)	37(1)	37(1)	37(1)	74(2)
t3	518(14)	296(8)	259(7)	185(5)	148(4)	111(3)	111(3)
t4 min	15						
t5 max	74(2)						
t6	37(1)						
t7	185(5)	111(3)	111(3)	111(3)	111(3)	74(2)	74(2)

Module Write Access

Memory write timings are valid for both attribute and common memory mode. IO and external device in regenerate mode share the same timing specifications as they all use IORD# and IOWR# signals. Timings are given in StarCI clock cycles. They are calculated to comply with PCMCIA specifications when 27 MHz clock is used.



Notes

(1) The WAIT/ACK output is either WAIT or ACK formatted according to the WAIT/ACK pin settings (driving structure, active level)

(2) Depending on the write access type, CE can be either CE1A# or CE1B# for access to memory or IO mode to module A or B, CE2A# or CE2B# for access in EC(Extended Channel) mode, or even EXTCS for access to external device in regenerate mode.

(3) REG# signal is not asserted during a common memory or external access.

(4) WE# signal is asserted during a memory access(attribute or common). It is replaced by IOWR# during an IO write cycle, an EC write cycle, or an external device in regenerate mode.

(5) t2 can be lengthened by the insertion of wait cycles. When the module asserts WAIT# signal, t2 cycles counter stops until WAIT# becomes inactive anew

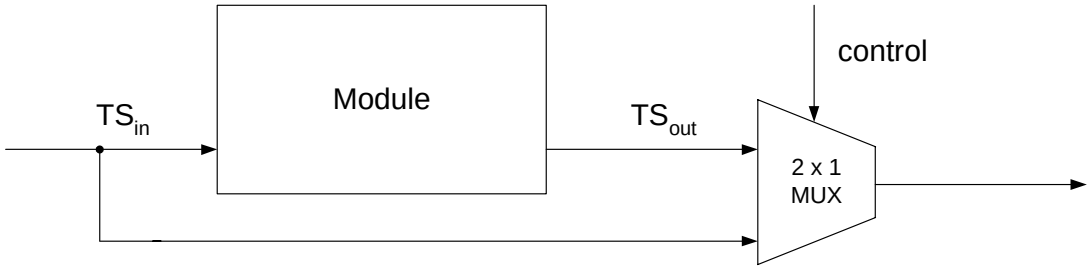
*unit:ns(cycle)

	Memory write					IO,EC, EXT
	600	250	200	150	100	
t0 max	15					
t1 max	74(2)					
t2	74(2)	37(1)				74(2)
t3	333(9)	185(5)	148(4)	111(3)	74(2)	185(5)
t4	74(2)	37(1)				37(1)
t5 max	15					

MPEG transport stream interface

TS bypass control

As a module can be inserted or removed at any time, the StarCI handles one MPEG transport stream bypass for each module. This bypass is enabled as long as a valid DVB CI module is not recognized to be inserted and activated in the corresponding slot or automatically as soon as the module is removed from a slot. The disabling of the bypass is controlled by the TSOEN bit in each Module Control Register.



TS/Addresses input signals

The MPEG input stream pins on the module are shared with the high order addresses specified by the PC card standard. When a module is inserted, before initialization, all these pins are forced to logical 0 state. If a memory module is recognized, the high order addresses A[25…15] can be applied to the module by setting the HAD bit in the Module Control Register. If a DVB module is recognized, the MPEG stream is applied to the module by setting the TSIEN bit in the Module Control Register. Those two bits cannot be set at the same time and are reset when the module is extracted. The TSOEN bit(TS bypass control bit) can only be set when TSIEN has previously been set. Resetting TSIEN also resets TSOEN.

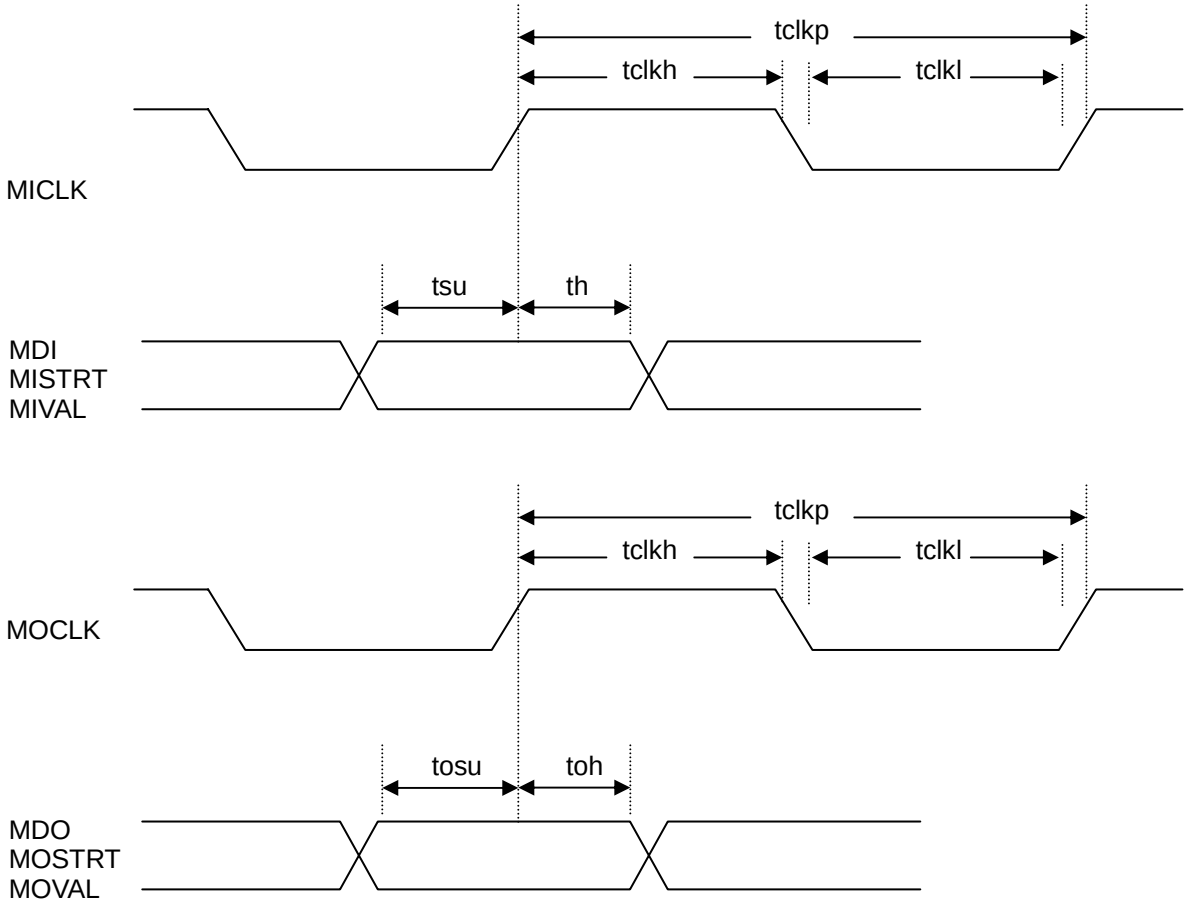
MPEG invert mask

Some modules can output an MPEG stream with inverted bits in the MPEG data bus. The StarCI is able to reinvert those bits to restore the correct data on the bus. This is achieved by setting the appropriate bits in the Invert Mask Register.

MPEG signals

The MPEG inputs of the StarCI should be connected to the MPEG source of the host or from another StarCI. MPEG signals coming from this source should respect the timing limits defined in the DVB standard. The MPEG outputs can be connected to any MPEG compliant destination or another StarCI. MPEG output signals are guaranteed to meet the provided timing specifications.

Definition of timings for TS signals



Timing diagram for transport stream interface

AC characteristics (VCC = 5V, T = 25 °C)

Item	Symbol	Min	Max
Clock period	tclkp	111 ns	
Clock high time	tclkh	40 ns	
Clock low time	tclkl	40 ns	
Input data setup	tsu	15 ns	
Input data hold	th	10 ns	
Output data setup	tosu	20 ns	
Output data hold	toh	15 ns	

Registers Description

StarCI includes several internal registers. All registers are reset to 00h. register bits marked X should not be set. Thev are read as 0.

Register Address	Description
00	Module A Control Register
01	Module A auto select mask high Register
02	Module A auto select mask low Register
03	Module A auto select pattern high Register
04	Module A auto select pattern low Register
05	Memory access A cycle time Register
06	Invert Input Mask A Register
07	RFU
08	RFU
09	Module B Control Register
0A	Module B auto select mask high Register
0B	Module B auto select mask low Register
0C	Module B auto select pattern high Register
0D	Module B auto select pattern low Register
0E	Memory access B cycle time Register
0F	Invert Input Mask B Register
10	RFU
11	RFU
12	External access auto select mask high Register
13	External access auto select mask low Register
14	External access auto select pattern high Register
15	External access auto select pattern low Register
16	RFU
17	Destination select Register
18	Power control Register
19	RFU
1A	Interrupt Status Register
1B	Interrupt Mask Register
1C	Interrupt Config Register
1D	Microprocessor Interface Config Register
1E	Microprocessor wait/ack Config Register
1F	StarCI Control Register

RFU : Reserved for Future Use

Register information

Address	Description
‘h00 (‘h09)	Module A (Module B) control register

RST	TSOEN	TSIEN	HAD	ACS1	ACS0	AUTO	DET

- RST
  RST pin control of common interface(CI) modules
  Only able to be set when DET=1
  Forced to 0 when DET=0
- TSOEN
  MPEG transport stream bypass control
  Only able to be set when DET=1 and HAD=0 and TSIEN=1
  Forced to 0 when DET=0 or TSIEN=0
  0 : bypass enabled
  1 : bypass disabled
- TSIEN
  MPEG transport stream input control
  Only able to be set when DET=1 and HAD=0
  Forced to 0 when DET=0
  0 : no MPEG stream
  1 : MPEG stream enabled
- HAD
  High order addresses in place of MPEG stream input
  Only able to be set when DET=1 and TSIEN=0 and TSOEN=0
  Forced to 0 when DET=0
  0 : apply MPEG stream
  1 : apply A[25:15] for memory access
- ACS[1:0]
  Module access type
  Only able to be set when DET=1
  Forced to “00” when DET=0
  00 : access to attribute memory
  01 : access to I/O space
  10 : access to common memory
- AUTO
  Module auto activation on detection
  0 : no auto activation procedure
  1 : start module auto activation when DET=1 if VCC=1
- DET
  Module detection
  0 : no module present
  1 : module inserted

‘h01 (‘h0A) Module A (Module B) auto select mask high register

X	X	X	X	X	MA25	MA24	MA23

‘h02 (‘h0B) Module A (Module B) auto select mask low register

MA22	MA21	MA20	MA19	MA18	MA17	MA16	MA15

- MA[25:15]
  Address mask for decoding
  0 : address bit doesn’t care
  1 : address bit should match programmed address bit in module auto select pattern register

‘h03 (‘h0C,’h14) Module A (Module B, External) auto select pattern high register

X	X	X	X	X	PA25	PA24	PA23

‘h04 (‘h0D,’h15) Module A (Module B, External) auto select pattern low register

PA22	PA21	PA20	PA19	PA18	PA17	PA16	PA15

- PA[25:15]
  Address pattern to match in accordance with address mask to select the corresponding module. Relevant only when DEF=0 in external auto select mask. Doesn’t care if DEF=1.

'h05 ('h0E) Module A (Module B) Memory access cycle time register

X	AM2	AM1	AM0	X	CM2	CM1	CM0

• AM[2:0] Attribute memory cycle time used

000 : 100ns
001 : 150ns
010 : 200ns
011 : 250ns
100 : 600ns

101 to 111 : reserved. Do not use

This timing is valid for write access. During read access, if AM=100, 600ns cycles will be used, if AM=0XX, 300ns will be used.

• CM[2:0] Common memory cycle time used

000 : 100ns
001 : 150ns
010 : 200ns
011 : 250ns
100 : 600ns

101 to 111 : reserved. Do not use

'h06 ('h0F) Module A (Module B) Invert input mask register

INV7	INV6	INV5	INV4	INV3	INV2	INV1	INV0

• INV[7:0]

Invert mask
0 : corresponding bit is not complemented
1 : corresponding bit is complemented

'h12 External access auto select mask high register

DEF	X	X	X	X	MA25	MA24	MA23

'h13 External access auto select mask low register

MA22	MA21	MA20	MA19	MA18	MA17	MA16	MA15

• DEF

External device default addressing
0 EXTCS asserted when address match mask and pattern
1 EXTCS asserted when neither module A nor module B is selected while CS input active

• MA[25:15]

Address mask for decoding
Relevant only when DEF=0. Doesn't care if DEF=1.
0 : address bit doesn't care
1 : address bit should match programmed address bit in module auto select pattern register

* 'h17 Destination select register

X	X	XCSDRV	XCSLVL	X	SEL1	SEL0	AUTOSEL

• XCSDRV

EXTCS output pin structure
Changing this bit is only allowed when LOCK=0
0 : EXTCS buffer is open-drain
1 : EXTCS buffer is push-pull

• XCSLVL

EXTCS output pin active level
Changing this bit is only allowed when LOCK=0
0 : EXTCS pin is active-low
1 : EXTCS pin is active-high

• SEL[1:0]

Module select
Relevant only when AUTOSEL=0
00 : no destination selected
01 : select module A
10 : select module B
11 : select external device using EXTCS

• AUTOSEL

Automatic module selection
Uses high order addresses to choose module or external device (using EXTCS)
0 : manual selection
1 : automatic selection

'h18 Power control register

VCDRV	VCLVL	X	X	X	X	X	VCC

- VCDRV
  Module VCC output pin structure
  Changing this bit is only allowed when LOCK=0
  0 : VCC buffer is open-drain
  1 : VCC buffer is push-pull

- VCLVL
  Module VCC output pin active level
  Changing this bit is only allowed when LOCK=0
  0 : VCC pin is active-low
  1 : VCC pin is active-high

- VCC
  Module power supply switch control
  Changing this bit is only allowed when LOCK=1
  0 : power off
  1 : power on

'h1A Interrupt status register

X	X	X	EXT	IRQB	IRQA	DETB	DETA

- EXT
  EXTINT status
  0 : EXTINT is inactive
  1 : EXTINT is active

- IRQB
  Slot B inverted IRQ line state
  0 : IRQ on slot B is high(inactive)
  1 : IRQ on slot B is low(active)

- IRQA
  Slot A inverted IRQ line state
  0 : IRQ on slot A is high(inactive)
  1 : IRQ on slot A is low(active)

- DETB
  Slot B module detection
  Reset on read
  0 : no change
  1 : a module has been inserted or extracted in slot B

- DETA
  Slot A module detection
  Reset on read
  0 : no change
  1 : a module has been inserted or extracted in slot A

'h1B Interrupt mask register

X	X	X	EXTM	IRQBM	IRQAM	DETBM	DETAM

- EXTM
  External interrupt mask
  0 : masked
  1 : unmasked : an interrupt request from external source will be transmitted to the microprocessor

- IRQBM
  Slot B IRQ mask
  0 : masked
  1 : unmasked : an interrupt request from module B will be transmitted to the microprocessor

- IRQAM
  Slot A IRQ mask
  0 : masked
  1 : unmasked : an interrupt request from module A will be transmitted to the microprocessor

- DETBM
  Slot B module detection mask
  Reset on read
  0 : masked
  1 : unmasked : a module movement in slot B will generate an interrupt

- DETAM
  Slot A module detection mask
  0 : masked
  1 : unmasked : a module movement in slot A will generate an interrupt

'h1C Interrupt configure register

X	X	X	X	X	ITDRV	ITLVL	EXTLVL

- ITDRV
  INT output pin structure
  Changing this bit is only allowed when LOCK=0
  0 : INT buffer is open-drain
  1 : INT buffer is push-pull

- ITLVL
  INT output pin active level
  Changing this bit is only allowed when LOCK=0
  0 : INT pin is active-low
  1 : INT pin is active-high

- EXTLVL
  EXTINT input pin active level
  Changing this bit is only allowed when LOCK=0
  0 : EXTINT pin is active-low
  1 : EXTINT pin is active-high

'h1D Microprocessor interface config register

X	X	X	X	CSLVL	WSTRLVL	RDIRLVL	RDIR

- CSLVL
  CS input active level
  Changing this bit is only allowed when LOCK=0
  0 : CS is active-low
  1 : CS is active-high

- WSTRLVL
  WR/STR input active level
  Changing this bit is only allowed when LOCK=0
  0 : WR/STR is active-low
  1 : WR/STR is active-high

- RDIRLVL
  RD/DIR input active level
  Changing this bit is only allowed when LOCK=0
  0 : RD is active-low or RD/DIR input is low during read transfer and high during write
  1 : RD is active-high or RD/DIR input is high during read transfer and high during write

- RDIR
  RD/DIR and WR/STR inputs function
  Changing this bit is only allowed when LOCK=0
  0 : RD/WR mode
  1 : DIR/STR mode

'h1E Microprocessor wait/ack config register

X	X	X	X	X	WACK	WDIR	WLVL

- WACK
  WAIT/ACK pin function
  Changing this bit is only allowed when LOCK=0
  0 : WAIT mode
  1 : ACK mode

- WDRV
  WAIT/ACK output pin structure
  Changing this bit is only allowed when LOCK=0
  0 : WAIT/ACK buffer is open-drain
  1 : WAIT/ACK buffer is push-pull

- WLVL
  WAIT/ACK output pin active level
  Changing this bit is only allowed when LOCK=0
  0 : WAIT/ACK pin is active-low
  1 WAIT/ACK pin is active-high

'h1F StarCI control register

RST	X	X	JCON	X	X	X	LOCK

- RST
  Reset chip
  1 : reset

- JCON
  Jitter Control mode select
  0 : jitter control mode off
  1 : jitter control mode on

- LOCK
  Validates and locks the chip setup
  0 : chip is not configured.
  1 : chip is configured

Electrical Characteristics

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Condition
	Power Supply	2.7V	3.6V	
V_{IL}	Input Low Level Voltage			Guaranteed Input Low Voltage
	CMOS input	-0.33V	$0.2xV_{DD}$	
	TTL input	-0.33V	0.8V	
V_{IH}	Input High Level Voltage			Guaranteed Input High Voltage
	CMOS input	$0.7xV_{DD}$	V_{DD}+0.5V	
	TTL input	2.0V	V_{DD}+0.5V	
	Junction Temperature	0℃	100℃	

DC Characteristics

Symbol	Parameter	Minimum		Maximum		Conditions	
		TTL	CMOS	TTL	CMOS	V_{DD}	
V_{IL}	Input Low Level Voltage	-0.5V	-0.5V	0.8V	$0.3xV_{DD}$	2.7V to 3.6V	Guaranteed Input Low Voltage
V_{IH}	Input High Level Voltage	2.0V	$0.7xV_{DD}$	V_{DD}+ 0.5V	V_{DD}+ 0.5V	2.7V to 3.6V	Guaranteed Input High Voltage
V_{OL}	Output Low Level Voltage			0.4V	V_{SS}+0.1V	2.7V	I_{OL} = 0.8mA(CMOS) I_{OL} = 2 to 0.8mA(TTL)
V_{OH}	Output High Level Voltage	2.4V	V_{DD}-0.1V			2.7V	I_{OH} = 0.8mA(CMOS) I_{OH} = 2 to 0.8mA(TTL)
I_I	Input Current at maximum voltage			1mA	1mA	2.7V to 3.6V	Input = 5.5V

I/O Circuit Pull ups & Pull downs

	Pull up I/Os		Pull down I/Os	
	Min (at pad = 0V)	Max (at pad = 0V)	Min (at pad =2.65V)	Max (at pad =2.65V)
Current	-30 μA	-146 μA	31 μA	159 μA
Equivalent resistance	88.3 kΩ	24.7 kΩ	85.5 kΩ	22.6 kΩ

Package Outline