■ MB8167A-55, MB8167A-70

NMOS 16,384-Bit Static Random Access Memory

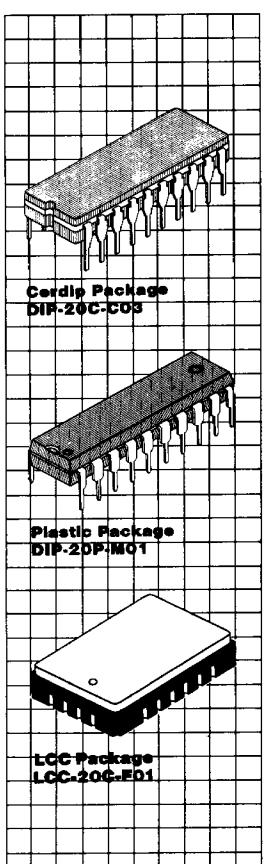
Description

The Fujitsu MB8167A is a 16,384 words by 1-bit static random access memory fabricated using N-channel silicon gate MOS technology. Separate input/output pins are provided. All devices are fully compatible with TTL logic families in all respects: inputs, output and the use of a single +5 V DC supply.

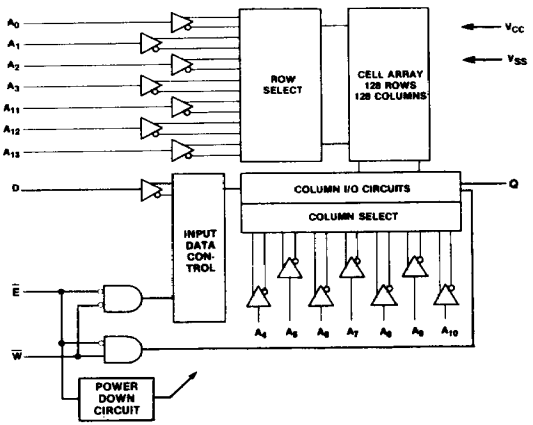
For ease of use, chip enable ($\overline{E}$) permits the selection of an individual package when outputs are OR-tied, and automatically powers down the MB8167A. This device offers the advantages of low power dissipation, low cost, and high performance.

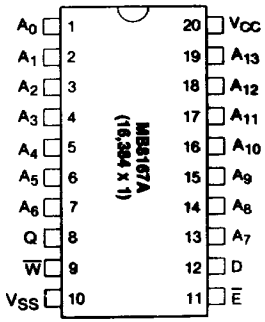
Features

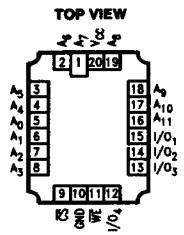
- Organized as 16,384 words x 1-bit
- Static operation: no clocks or refresh required
- Fast Access Time:
  MB8167A-55 55 ns Max.
  MB8167A-70 70 ns Max.
- Single +5 V DC supply voltage
- Separate data input and output
- TTL compatible inputs and output
- Three-state output with OR-tie capability
- Chip enable for simplified memory expansion and automatic power down
- All inputs and output have protection against static charge
- Standard 20-pin DIP package



MB8167A Block Diagram and Pin Assignment







(LCC-20C-F01)

Truth Table

$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Voltage On Any Pin with Respect to V_{SS}		VIN, VOUT, VCC	−3.5 to +7	V
Temperature Under Bias		TA	−10 to +85	°C
Storage Temperature	Ceramic	TSTG	−65 to +150	°C
	Plastic	TSTG	−40 to +125	
Power Dissipation		PD	1.2	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance
(T_A = 25°C; f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN = 0V)	CIN	—	5	pF
Output Capacitance (VOUT = 0V)	COUT	—	6	pF

Recommended Operating Conditions
(Referenced to VSS)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient[1] Temperature
Supply Voltage	VCC	4.5	5.0	5.5	V	0°C to +70°C
Input Low Voltage	VIL	−3.0[2]	—	0.8	V	
Input High Voltage	VIH	2.0	—	6.0	V	

Note: (1) The operating ambient temperature range is guaranteed with transverse airflow exceeding 2 linear meters/second.
(2) −3.0 V Min. for pulse width less than 20 ns. (V_{IL} Min. = −0.5 at DC level)

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

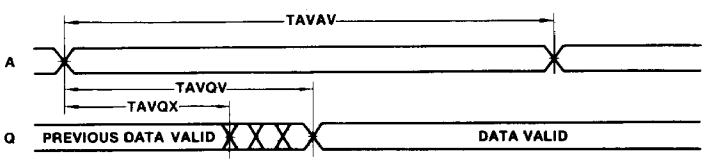
Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (VIN = VSS to VCC, VCC = Max)	ILI	—	0.01	10	μA
Output Leakage Current $\overline{E}$ = VIH, VOUT = VSS to VCC Min, VCC = Max)	I_{LO}	—	0.1	50	μA
Power Supply Current (VCC = Max, $\overline{E}$ = VIL, IOUT = 0mA)	ICC	—	90	120	mA
Output Low Voltage (IOL = 16mA)	VOL	—	—	0.45	V
Output High Voltage (IOH = −4mA)	VOH	2.4	—	—	V
Standby Current (VCC = Min to Max, $\overline{E}$ = VIH	ISB	—	15	25	mA
Peak Power-On Current (VCC = VSS to VCC Min, $\overline{E}$ = Lower of VCC or VIH Min)	IPO	—	—	25	mA

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

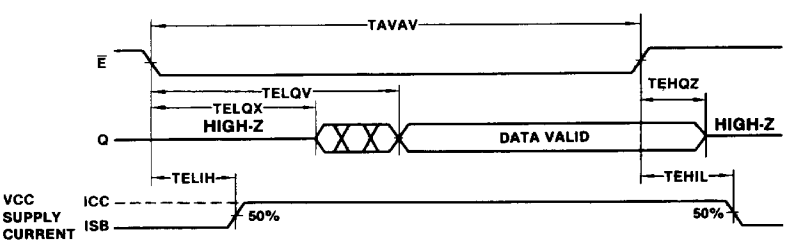
Read Cycle

Parameter	Notes	Symbol	MB8167A-55 Min	MB8167A-55 Max	MB8167A-70 Min	MB8167A-70 Max	Unit
Read Cycle Time		TAVAV	55	—	70	—	ns
Address Access Time		TAVQV		55		70	ns
Chip Enable Access Time		TELQV	—	55	—	70	ns
Output Hold from Address Change		TAVQX	5	—	5	—	ns
Chip Enable to Output Active	1 2	TELQX	10	—	10	—	ns
Chip Enable to Output in High Z	1 2	TEHQZ	0	30	0	40	ns
Chip Enable to Power Up Time		TELIH	0	—	0	—	ns
Chip Enable to Power Down Time		TEHIL	—	30	—	35	ns

Read Cycle: Address Controlled [3,4]



Read Cycle: $\overline{E}$ Controlled [3, 5]



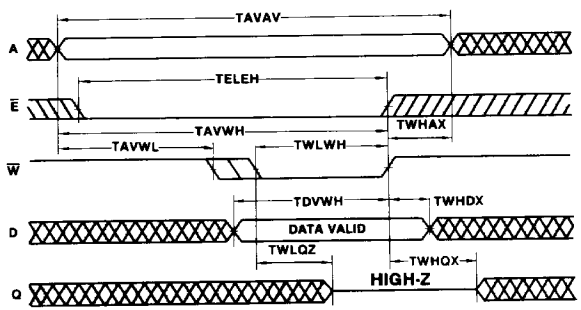
Notes:
1. Transition is measured at the point of ±500mV from steady state voltage.
2. This parameter is measured with specified loading in Fig.2.
3. $\overline{W}$ is high for Read Cycle.
4. Device is continuously selected, $\overline{E}$ = VIL.
5. Addresses valid prior to or coincident with $\overline{E}$ transition low.

AC Characteristics
(Recommended operating conditions unless otherwise noted.) (continued)

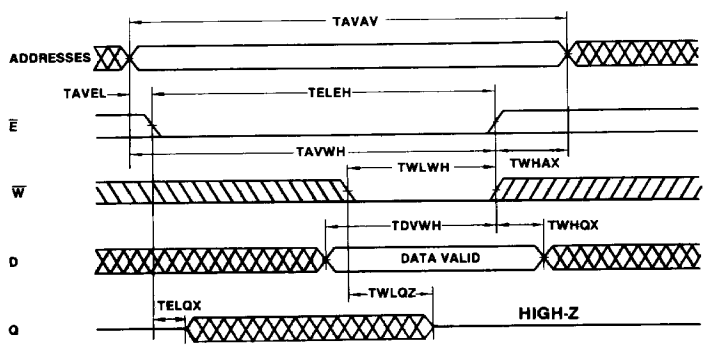
Write Cycle

Parameter	Notes	Symbol	MB8167A-55 Min	MB8167A-55 Max	MB8167A-70 Min	MB8167A-70 Max	Unit
Write Cycle Time		TAVAV	55	—	70	—	ns
Address Valid to End of Write		TAVWH	45	—	50	—	ns
Chip Enable to End of Write		TELEH	50	—	60	—	ns
Data Valid to End of Write		TDVWH	35	—	45	—	ns
Data Hold Time		TWHDX	0	—	0	—	ns
Write Pulse Width		TWLWH	35	—	45	—	ns
Write Recovery Time		TWHAX	5	—	10	—	ns
Address Setup Time		TAVWL	5	—	10	—	ns
		TAVEL	0	—	0	—	ns
Output Active From End of Write	7, 8	TWHQX	0	—	0	—	ns
Write Enable to Output in High Z	7, 8	TWLQZ	—	30	—	35	ns

Write Cycle: $\overline{W}$ Controlled[6,9]



Write Cycle: $\overline{E}$ Controlled[6,9]

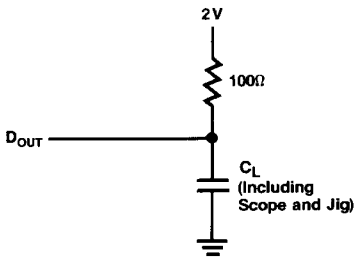


Notes:
6. If $\overline{E}$ goes high simultaneously with $\overline{W}$ high, the output remains in a high impedance state.
7. Transition is measured at the point of ±500mV from steady state voltage.
8. This parameter is measured with specified loading in Fig. 2.
9. $\overline{E}$ or $\overline{W}$ must be high during address transitions.

AC Test Conditions

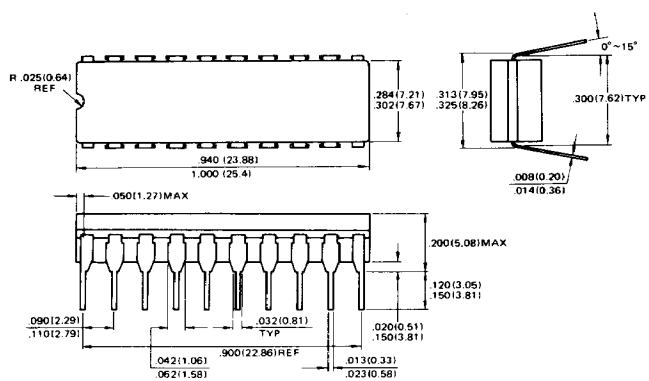
Input Pulse Levels:	0.8 V to 2.2 V
Input Pulse Rise and Fall Times:	5 ns
Timing Measurement Reference Levels:	Inputs: 1.5 V Output: 1.5 V
Load Capacitance:	5 pF for TEHQZ, TWLQZ, TELQX and TWHQX 30 pF for all others

Fig. 2: Output Load



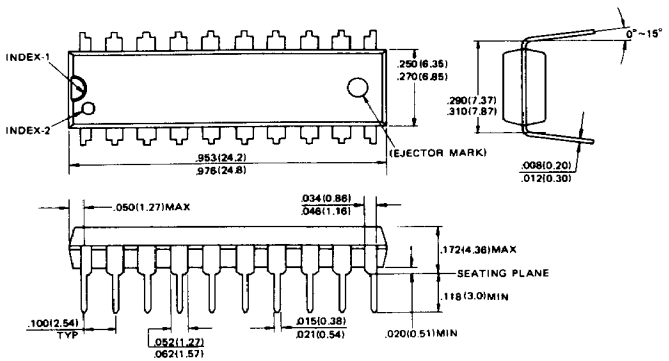
Package Dimensions
Dimensions in inches
(millimeters)

20-Lead Cerdip
Dual In-Line Package
DIP-20C-C03



Package Dimensions
Dimensions in inches (millimeters) (continued)

20-Lead Plastic Dual In-Line Package DIP-20P-M01



20-Pad Ceramic (Frit Seal) Leadless Chip Carrier (Case No.: LCC-20C-F01)