Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (8K x 8-BIT) CACHE-TAG RAM

IDT7174S
NOT RECOMMENDED FOR NEW DESIGNS
SEE IDT71B74 PAGE 6.15

FEATURES:

- High-speed address to MATCH comparison time
  - — Military: 35/45/55ns (max.)
  - — Commercial: 30/35/45ns (max.)
- High-speed address access time
  - — Military: 35/45/55ns (max.)
  - — Commercial: 30/35/45ns (max)
- High-speed chip select access time
  - — Military: 20/25/30ns (max.)
  - — Commercial: 15/20/25ns (max.)
- Low-power operation
  - — IDT7174S
    Active: 300mW (typ.)
- High-speed asynchronous RAM Clear on Pin 1 (Reset Cycle Time = 2 x t_{AA})
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (+10%) power supply
- Input and output directly TTL-compatible
- Military product compliant to MIL-STD-883, Class B
- Standard 28-pin plastic DIP (600 mil), 28-pin SOIC (330 mil gull-wing), 28-pin hermetic DIP (300 mil or 600 mil), 32-pin LCC and PLCC
- Not recommended for new designs. See FDT71B74, page 6.15

DESCRIPTION:

The IDT7174 is a high-speed cache address comparator subsystem consisting of a 65,536-bit static RAM organized as 8K x 8 and an 8-bit comparator. A single IDT7174 can map 8K cache words into a 1 megabyte address space by comparing 20 bits of address organized as 13 word cache address bits and 7 upper address bits. Two IDT7174s can be combined to provide 28 bits of address comparison, etc. The IDT7174 also provides a single RAM clear control, which clears all words in the internal RAM to zero when activated. This allows the tag bits for all locations to be cleared at power-on or system-reset, a requirement for cache comparator systems.

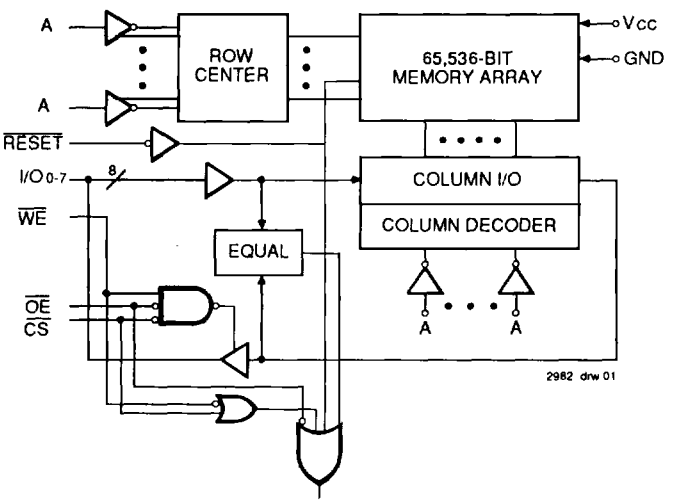
The IDT7174 is fabricated using IDT's high-performance, high-reliability technology — CEMOS. Address access times as fast as 30ns, chip select times of 15ns and address-to-comparison times of 30ns are available with maximum power consumption of 825mW.

All inputs and outputs of the IDT7174 are TTL-compatible. The MATCH pin of several 7174's can be wired-ORed together to provide enabling or acknowledging signals to the data cache or processor, thus eliminating logic delays and increasing system throughput. The device operates from a single 5V supply.

The IDT7174 is packaged in a 28-pin DIP (600 mil and 300 mil), a 28-pin SOIC (gull-wing) and 32-pin LCC and PLCC, providing high board level packing densities.

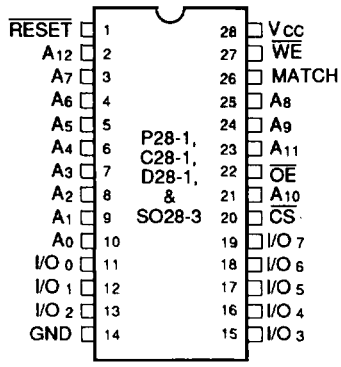
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



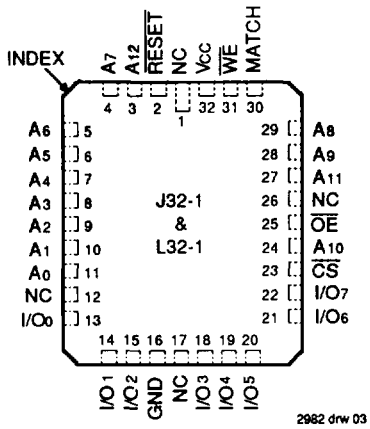
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



2982 drw 02

DIP/SOIC TOP VIEW



2982 drw 03

LCC/PLCC TOP VIEW

TRUTH TABLE[1]

WE	CS	OE	RESET	MATCH	I/O	Function
X	X	X	L	H	—	Reset all bits to low
X	H	X	H	H	Hi Z	Deselect chip
H	L	H	H	L	DIN	No MATCH
H	L	H	H	H	DIN	MATCH
H	L	L	H	H	DOUT	Read
L	L	X	H	H	DIN	Write

NOTE: 2982 tbl 01
1. H = VIH, L = VIL, X = don't care.

PIN DESCRIPTIONS

A0–12	Address
I/O0–7	Data Input/Output
CS	Chip Select
RESET	Memory Reset
MATCH	Data/Memory Match (Open Drain)
WE	Write Enable
OE	Output Enable
GND	Ground
VCC	Power

2982 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE: 2982 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE: 2982 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

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RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage[1]	2.2	—	6.0	V
V_{IHR}	$\overline{RESET}$ Input Voltage	2.5[2]	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[3]	—	0.8	V

NOTES: 2982 tbl 05

1. All inputs except $\overline{RESET}$.
2. When using bipolar devices to drive the $\overline{RESET}$ input, a pullup resistor of 1kΩ-10kΩ is usually required to assure this voltage.
3. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V_{CC}
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2982 tbl 06

DC ELECTRICAL CHARACTERISTICS[1,2]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	7174S30		7174S35		7174S45		7174S55		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current Outputs Open, V_{CC} = Max., f = 0	110	—	110	125	110	125	—	125	mA
I_{CC2}	Dynamic Operating Current Outputs Open, V_{CC} = Max., f = f_{MAX}	170	—	150	170	140	150	—	145	mA

NOTES: 2982 tbl 07

1. All values are maximum guaranteed values.
2. f = MAX. means that address and data are cycling at maximum frequency of read cycles of 1/t_{RC}.
   f = 0 means no inputs change.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition		IDT7174S Min.	IDT7174S Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	—	10	µA
			COM'L.	—	5	
$\|I_{LO}\|$	Output Leakage Current[1]	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	10	µA
			COM'L.	—	5	
V_{OL}	Output Low Voltage	I_{OL} = 18mA MATCH		—	0.5	V
		I_{OL} = 22mA MATCH		—	0.5	
		I_{OL} = 10mA, V_{CC} = Min. (Except MATCH)		—	0.5	
		I_{OL} = 8mA, V_{CC} = Min. (Except MATCH)		—	0.4	
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min. (Except MATCH)		2.4	—	V

NOTE: 2992 tbl 08

1. Data and MATCH pins.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 and 3

2982 tbl 09

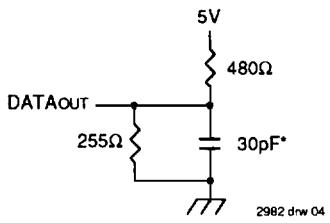


Figure 1. Output Load

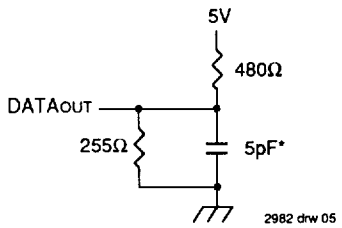
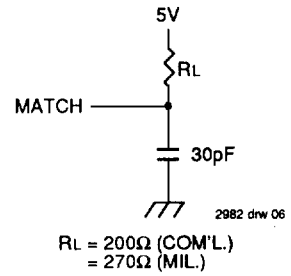


Figure 2. Output Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, tWHZ)

*Includes scope and jig.



RL = 200Ω (COM'L.)
= 270Ω (MIL.)

Figure 3. Output Load for MATCH

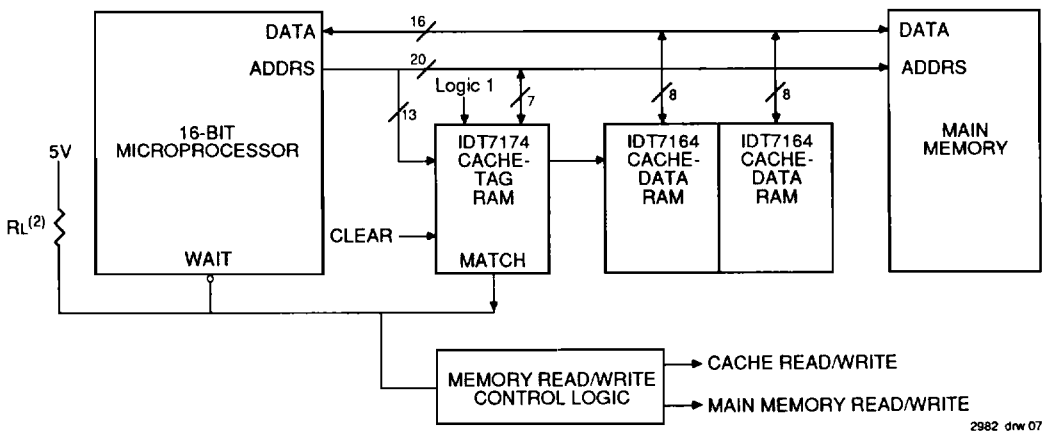


Figure 4. Example of Cache Memory System Block Diagram

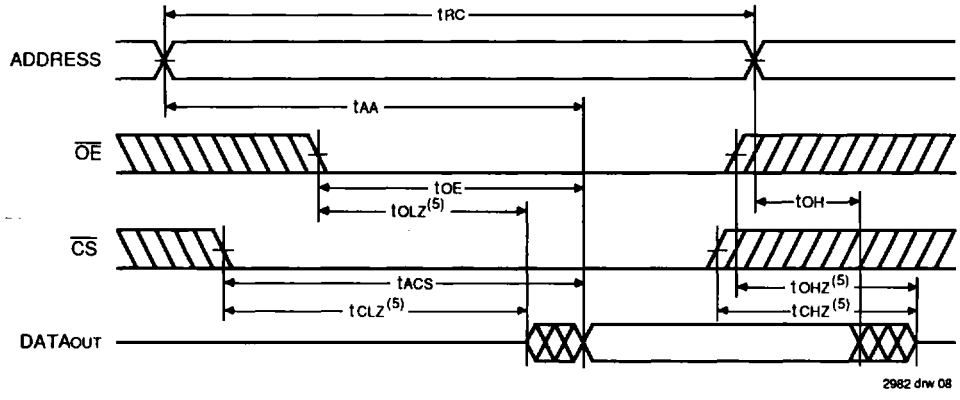
NOTES:
1. For more information, see application note AN-07 "Cache-Tag RAM Chips Simplify Cache Memory Design".
2. RL = 200Ω (commercial) or 270Ω (military).

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7174S30[1]		7174S35		7174S45		7174S55[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	30	—	35	—	45	—	55	—	ns
tAA	Address Access Time	—	30	—	35	—	45	—	55	ns
tACS	Chip Select Access Time	—	18	—	20	—	25	—	30	ns
tCLZ	Chip Select to Output in Low Z[3]	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	—	18	—	20	—	25	—	30	ns
tOLZ	Output Enable to Output in Low Z[3]	3	—	3	—	3	—	3	—	ns
tCHZ	Chip Select to Output in High Z[3]	—	15	—	15	—	20	—	25	ns
tOHZ	Output Disable to Output in High Z[3]	—	15	—	15	—	20	—	25	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns

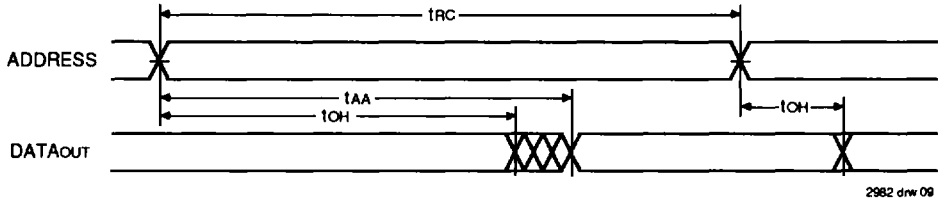
NOTES:
2982 tbl 10
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed, but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



2982 drw 08

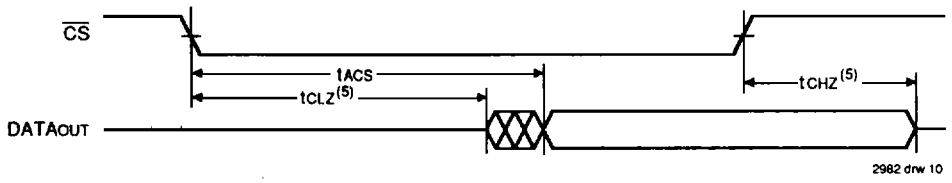
TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]



2982 drw 09

NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7174S30(1)		7174S35		7174S45		7174S55(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
tWC	Write Cycle Time	30	—	35	—	45	—	55	—	ns
tCW	Chip Select to End of Write	18	—	20	—	25	—	30	—	ns
tAW	Address Valid to End of Write	25	—	30	—	40	—	50	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	25	—	30	—	40	—	50	—	ns
tWR	Write Recovery Time ($\overline{CS}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High Z(3)	—	15	—	15	—	20	—	25	ns
tDW	Data to Write Time Overlap	14	—	15	—	20	—	25	—	ns
tDH	Data Hold from Write Time	2	—	2	—	2	—	2	—	ns
tOW	Output Active from End of Write(3)	5	—	5	—	5	—	5	—	ns

NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed, but not tested.

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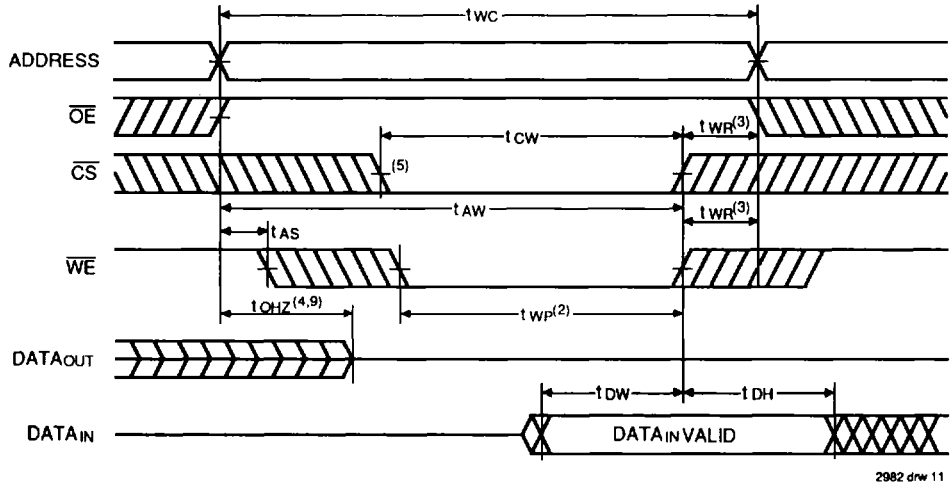
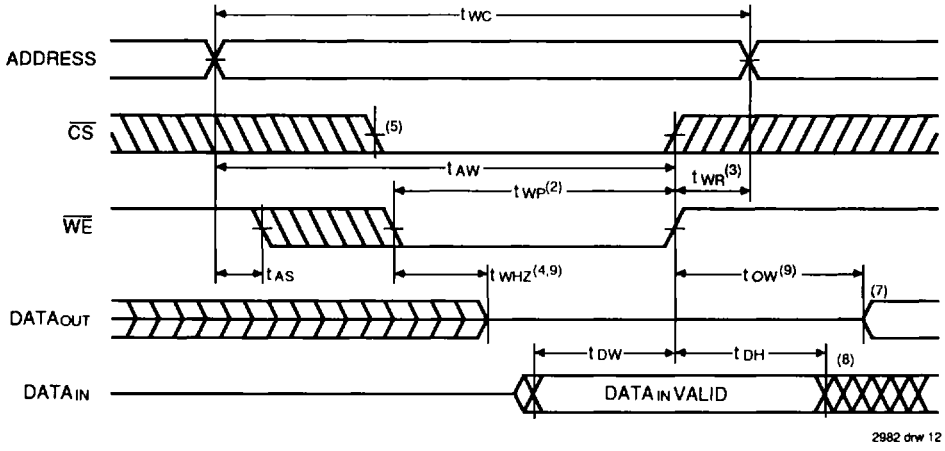
TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2(1, 6)



NOTES:
1. $\overline{WE}$, $\overline{CS}$ must be inactive during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{WE}$ and a low $\overline{CS}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. If $\overline{OE}$ is continuously low ($\overline{OE}$ = VIL).
7. DATAOUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state.

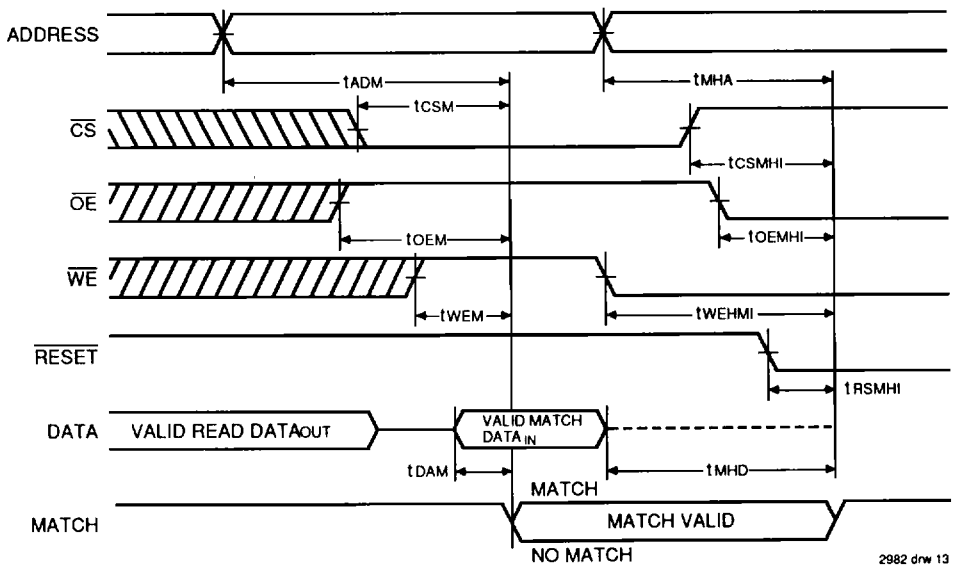
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7174S30[1] Min.	7174S30[1] Max.	7174S35 Min.	7174S35 Max.	7174S45 Min.	7174S45 Max.	7174S55[2] Min.	7174S55[2] Max.	Unit
Match Cycle										
tADM	Address to MATCH Valid	—	30	—	35	—	45	—	55	ns
tCSM	Chip Select to MATCH Valid	—	18	—	20	—	25	—	30	ns
tCSMHI	Chip Select to MATCH High	—	18	—	20	—	25	—	30	ns
tDAM	Data Input to MATCH Valid	—	23	—	25	—	35	—	45	ns
tOEMHI	$\overline{OE}$ Low to MATCH Hgih	—	23	—	25	—	35	—	45	ns
tOEM	$\overline{OE}$ High to MATCH Valid	—	23	—	25	—	35	—	45	ns
tWEMHI	$\overline{WE}$ Low to MATCH High	—	23	—	25	—	35	—	45	ns
tWEM	$\overline{WE}$ High to MATCH Valid	—	23	—	25	—	35	—	45	ns
tRSMHI	$\overline{RESET}$ Low to MATCH High	—	23	—	25	—	35	—	45	ns
tMHA	MATCH Valid Hold From Address	5	—	5	—	5	—	5	—	ns
tMHD	MATCH Valid Hold From Data	5	—	5	—	5	—	5	—	ns

2982 tbl 12

NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.

MATCH TIMING[1]



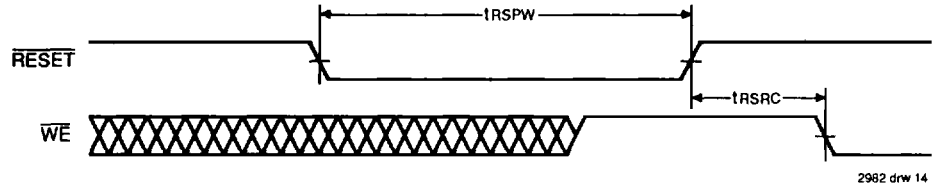
NOTE:
1. It is not recommended to float the data and address inputs of this device while the MATCH pin is active.

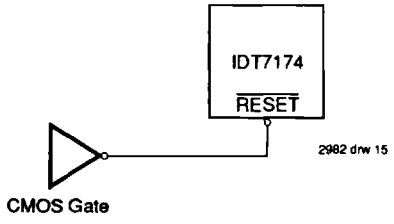
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7174S30[1]		7174S35		7174S45		7174S55[3]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRSPW	Reset Pulse Width[2]	55	—	65	—	80	—	100	—	ns
tRSRC	Reset High to $\overline{WE}$ Low	5	—	5	—	10	—	10	—	ns

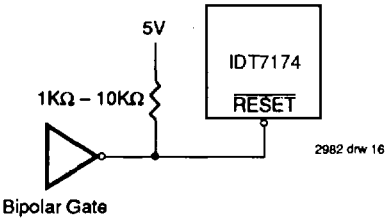
NOTES:
1. 0° to +70°C temperature range only.
2. Recommended duty cycle = 10% maximum.
3. -55°C to +125°C temperature range only.

RESET TIMING





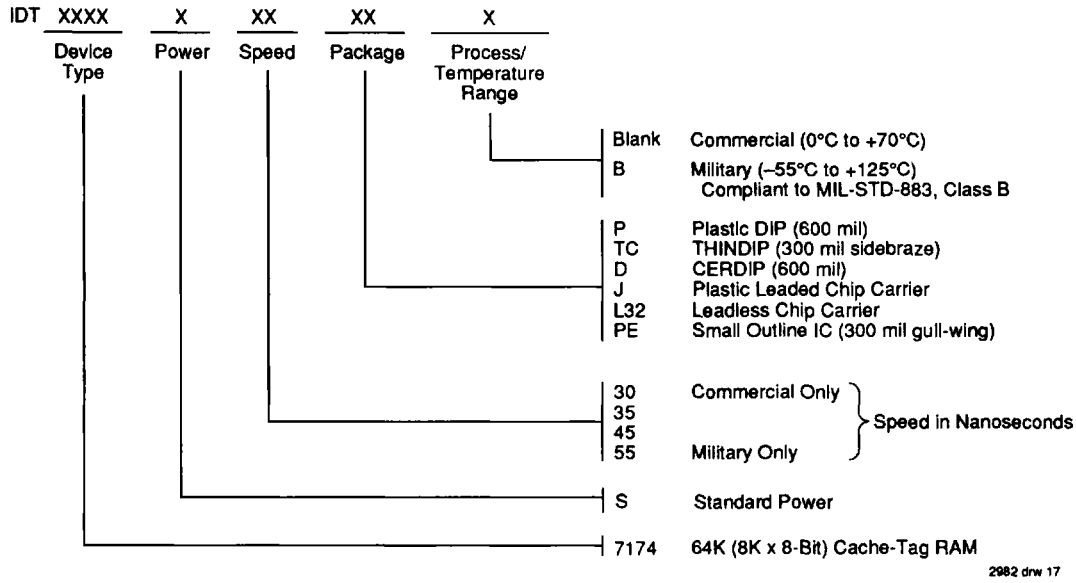
Driving the $\overline{RESET}$ pin with CMOS logic.



Driving the $\overline{RESET}$ pin with bipolar logic.

Figure 5.

ORDERING INFORMATION



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