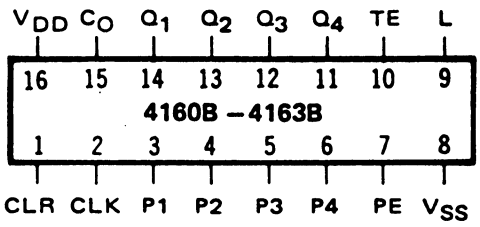
CMOS SYNCHRONOUS 4-BIT COUNTERS

FEATURES

- BCD Decade (4160B, 4162B) or 4-Bit Binary (4161B, 4163B) Counting
- Internal Look-Ahead for Fast Counting
- Carry Output for Cascading
- Synchronously Programmable
- Sychronous Counting
- Load Control Input
- Clear Input - Asynchronous (4160B, 4161B) or Synchronous (4162B, 4163B)
- Static Operation - DC to 5MHz @ 10Vdc

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C 16-pin Cerdip

E 16-pin Epoxy

DESCRIPTION

The 4160B - 4163B are Synchronous Programmable Counters constructed with complementary MOS P-Channel and N-Channel enhancement-mode devices in a single monolithic structure. These counters are functionally equivalent to the 74160 - 74163 TTL counters.

Two are synchronous programmable decade counters with asynchronous and synchronous Clear inputs respectively (4160, 4162). The other two are 4-bit binary counters with asynchronous and synchronous Clear respectively (4161, 4163).

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C		-55 to +125	°C
E		-40 to +85	°C

SYNCHRONOUS MODE SELECTION
4160B/4161B

L	PE	TE	Mode
L	X	X	Preset
H	L	X	No Change
H	X	L	No Change
H	H	H	Count

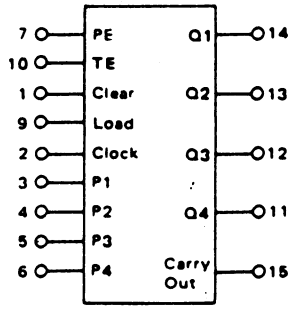
H = High level L = Low level X = Don't care

SYNCHRONOUS MODE SELECTION
4162B/4163B

CLR	L	PE	TE	Mode
H	L	X	X	Preset
H	H	L	X	No Change
H	H	X	L	No Change
H	H	H	H	Count
L	X	X	X	Reset

H = High level L = Low level X = Don't care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

SELECTOR GUIDE

CLEAR	MODULUS	
	DECADE	BINARY
Asynchronous	4160B	4161B
Synchronous	4162B	4163B

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C
= -40°C for E
T_{HIGH} = +125°C for C
= + 85°C for E

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

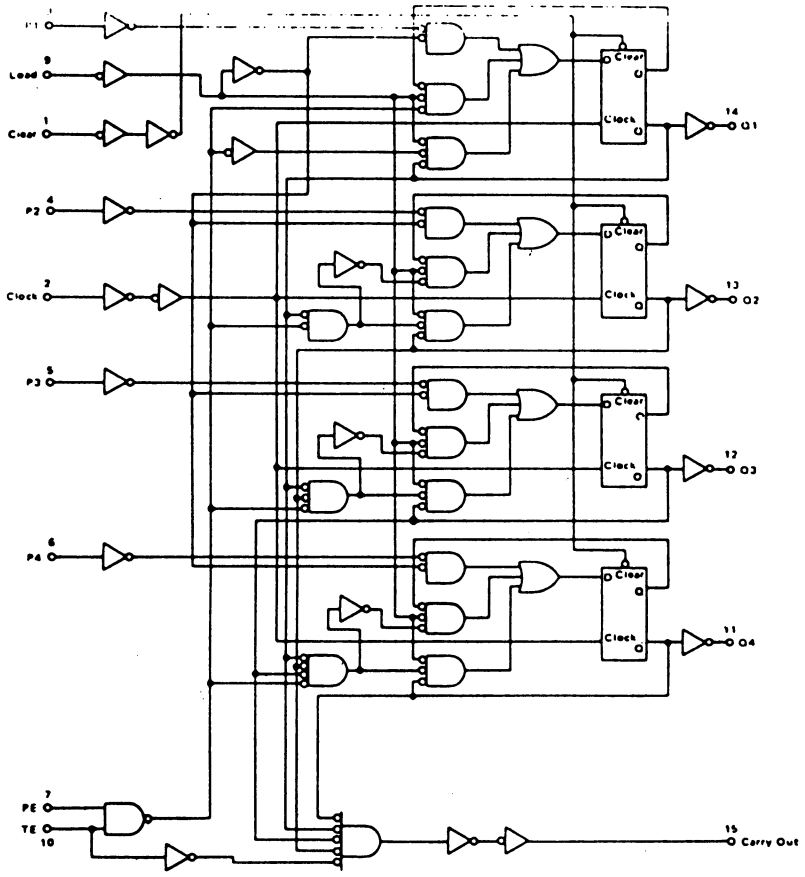
PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Q	t_{PLH}, t_{PHL}	5	–	200	400	ns
		10	–	80	160	
		15	–	60	120	
Clock to Carry Out		5	–	240	480	ns
		10	–	95	190	
		15	–	75	150	
TE to Carry Out		5	–	180	360	ns
		10	–	70	140	
		15	–	50	100	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	85	170	ns
		10	–	35	70	
		15	–	25	50	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	2.0	3.0	–	MHz
		10	5.5	8.5	–	
		15	8.0	12.0	–	
MAXIMUM CLOCK RISE AND FALL TIME[1]	t_{rCL}, t_{fCL}	5	50	∞	–	ms
		10	50	∞	–	
		15	50	∞	–	
MINIMUM SETUP TIME Data to Clock	t_{setup}	5	–	120	240	ns
		10	–	45	90	
		15	–	30	65	
Load to Clock		5	–	120	240	ns
		10	–	45	90	
		15	–	30	65	
PE or TE to Clock		5	–	170	340	ns
		10	–	70	140	
		15	–	50	100	
CLEAR OPERATION						
PROPAGATION DELAY TIME Clear to Q (4160, 4161 only)	t_{PLH}, t_{PHL}	5	–	150	300	ns
		10	–	50	100	
		15	–	30	60	
MINIMUM SETUP TIME Clear to Clock (4162, 4163 only)	t_{setup}	5	–	120	240	ns
		10	–	50	100	
		15	–	30	60	

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

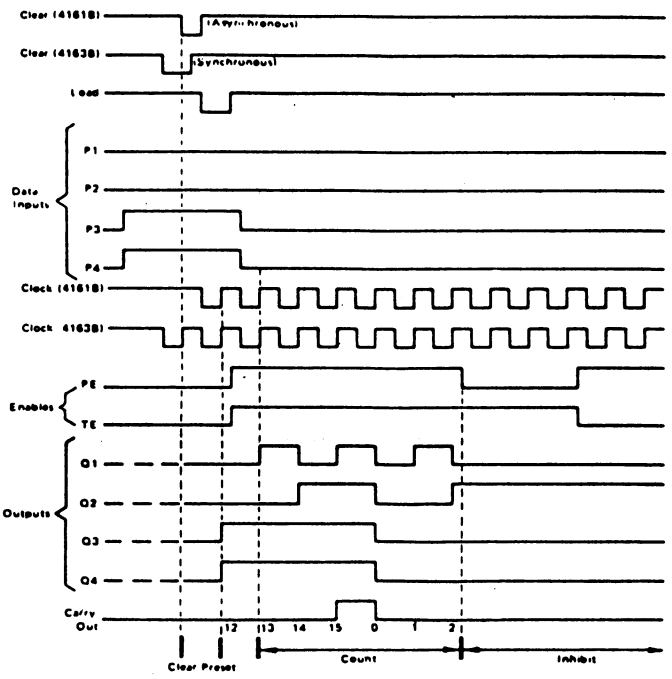
4161B, 4163B LOGIC DIAGRAM
(Clear is Synchronous for 4163B)

Sequence illustrated in waveforms:

1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one and two.
4. Inhibit.



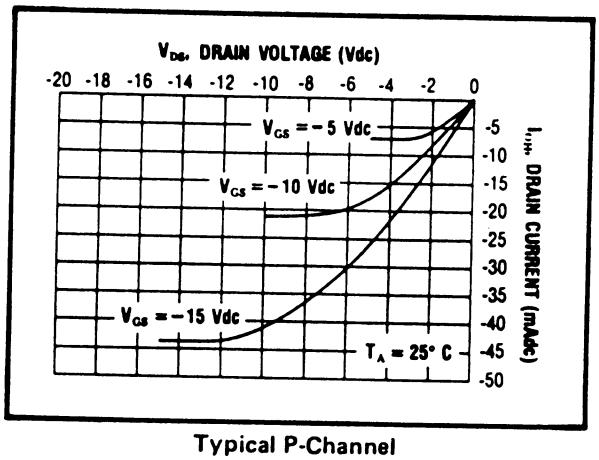
4161B, 4163B TIMING DIAGRAM



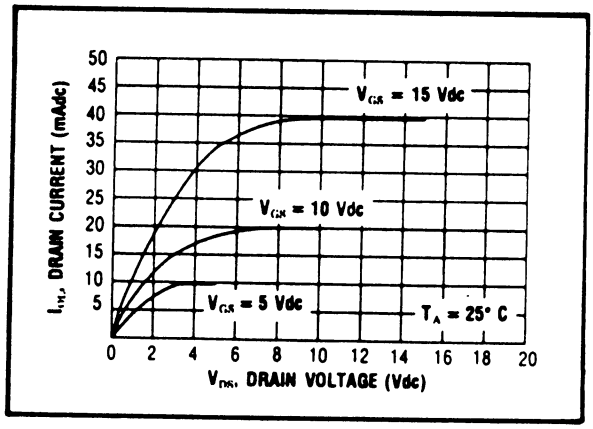
FUNCTIONAL DESCRIPTION

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the Load input disables the counter and causes the outputs to agree with the setup data after the next Clock pulse regardless of the levels of the Enable inputs. Low-to-high transitions at the Load input should be avoided when the Clock is low if the Enable inputs are high at or before the transition. The Clear function for the 4160, 4161 is asynchronous and a low level at the Clear input sets all four of the flip-flop outputs low regardless of the levels of the Clock, Load or Enable inputs. The Clear function for the 4162 and 4163 is synchronous and a low level at the Clear inputs sets all four of the flip-flop outputs low after the next Clock pulse regardless of the levels of the Enable inputs. This synchronous Clear allows the count length to be modified easily; decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the Clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs and a Carry output. Both Count Enable inputs (PE, TE) must be high to count, and Enable input TE is fed forward to enable the carry output. The Carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow Carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the Enable PE or TE inputs should occur only when the Clock input is high.



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

SWITCHING WAVEFORMS