

PROTECTION PRODUCTS

Description

The LCDA series of TVS arrays are designed to protect sensitive electronics from damage or latch-up due to ESD and other voltage-induced transient events. Each device will protect two high-speed lines. They are available with operating voltages of 5V, 12V, 15V and 24V. They are bidirectional devices and may be used on lines where the signal polarities are above and below ground.

TVS diodes are solid-state devices designed specifically for transient suppression. They offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage and no device degradation. The LCDA series devices feature low capacitance compensation diodes in series with standard TVS diodes to provide an integrated, low capacitance solution for use on high-speed interfaces.

The LCDA series devices may be used to meet the immunity requirements of IEC 61000-4-2, level 4.

Features

- ◆ Transient protection for high-speed data lines to **IEC 61000-4-2 (ESD) 15kV (air), 8kV (contact)**
IEC 61000-4-4 (EFT) 40A (tp = 5/50ns)
IEC 61000-4-5 (Lightning) 24A (tp = 8/20µs)
- ◆ Protects two I/O lines
- ◆ Low capacitance for high-speed data lines
- ◆ Working voltages: 5V, 12V, 15V and 24V
- ◆ Low leakage current
- ◆ Low operating and clamping voltages
- ◆ Solid-state silicon avalanche technology

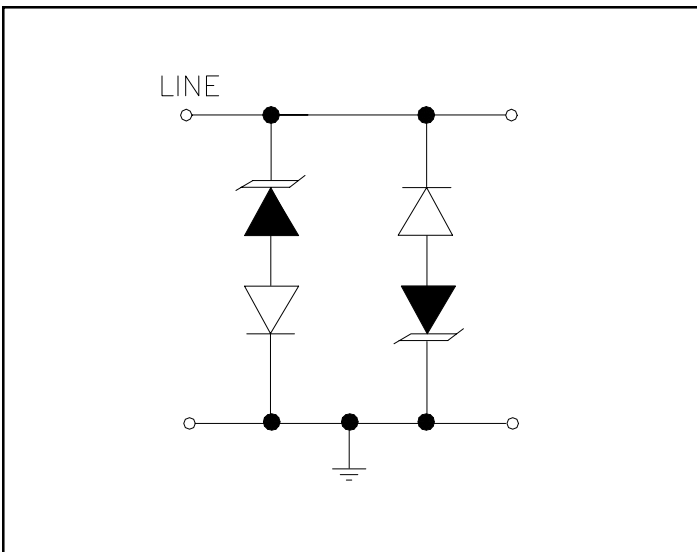
Mechanical Characteristics

- ◆ JEDEC SO-8 (MS-012AA) small outline package
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking : Part Number, Logo, Date Code
- ◆ Packaging : Tape and Reel per EIA 481

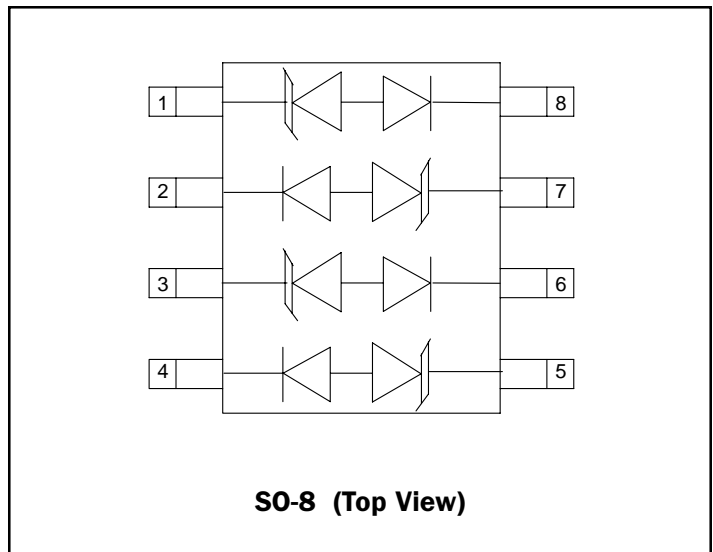
Applications

- ◆ High-Speed Data Lines
- ◆ Microprocessor Based Equipment
- ◆ Universal Serial Bus (USB) Port Protection
- ◆ Notebooks, Desktops, & Servers
- ◆ Instrumentation
- ◆ LAN/WAN Equipment
- ◆ Peripherals

Circuit Diagram (Each Line Pair)



Schematic & PIN Configuration



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Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P_{pk}	300	Watts
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics

LCDA05						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$	6			V
Reverse Leakage Current	I_R	$V_{RWM} = 5V, T=25^\circ C$			20	μA
Clamping Voltage	V_C	$I_{PP} = 1A, tp = 8/20\mu s$			9.8	V
Clamping Voltage	V_C	$I_{PP} = 5A, tp = 8/20\mu s$			11	V
Junction Capacitance	C_j	Between I/O Pins and Gnd $V_R = 0V, f = 1MHz$			5	pF

LCDA12						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				12	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$	13.3			V
Reverse Leakage Current	I_R	$V_{RWM} = 12V, T=25^\circ C$			1	μA
Clamping Voltage	V_C	$I_{PP} = 1A, tp = 8/20\mu s$			19	V
Clamping Voltage	V_C	$I_{PP} = 5A, tp = 8/20\mu s$			24	V
Junction Capacitance	C_j	Between I/O Pins and Gnd $V_R = 0V, f = 1MHz$			5	pF

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Electrical Characteristics (continued)

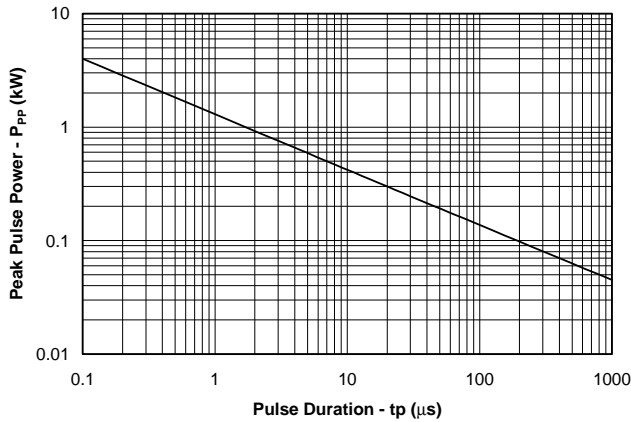
LCDA15						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				15	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$	16.7			V
Reverse Leakage Current	I_R	$V_{RWM} = 15V, T=25^\circ C$			1	μA
Clamping Voltage	V_C	$I_{PP} = 1A, tp = 8/20\mu s$			24	V
Clamping Voltage	V_C	$I_{PP} = 5A, tp = 8/20\mu s$			30	V
Junction Capacitance	C_j	Between I/O Pins and Gnd $V_R = 0V, f = 1MHz$			5	pF

LCDA24						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				24	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$	26.7			V
Reverse Leakage Current	I_R	$V_{RWM} = 24V, T=25^\circ C$			1	μA
Clamping Voltage	V_C	$I_{PP} = 1A, tp = 8/20\mu s$			43	V
Clamping Voltage	V_C	$I_{PP} = 5A, tp = 8/20\mu s$			55	V
Junction Capacitance	C_j	Between I/O Pins and Gnd $V_R = 0V, f = 1MHz$			5	pF

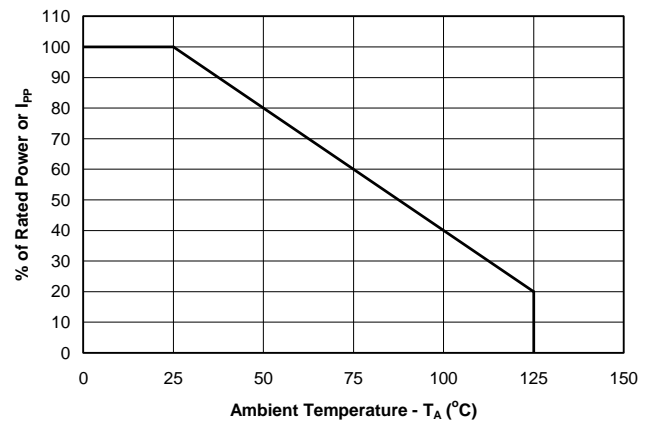
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Typical Characteristics

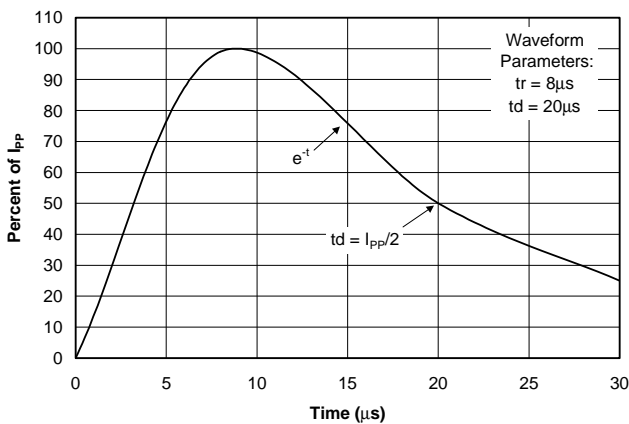
Non-Repetitive Peak Pulse Power vs. Pulse Time



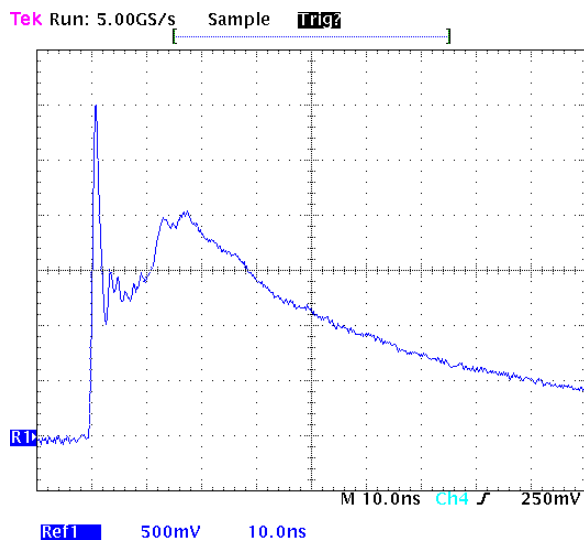
Power Derating Curve



Pulse Waveform



ESD Pulse Waveform (Per IEC 61000-4-2)



ESD Discharge Parameters Per IEC 61000-4-2

Level	First Peak Current (A)	Peak Current at 30ns (A)	Peak Current at 60ns (A)	Test Voltage (Contact Discharge) (kV)	Test Voltage (Air Discharge) (kV)
1	7.5	4	8	2	2
2	15	8	4	4	4
3	22.5	12	6	6	8
4	30	16	8	8	15

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Applications Information

Device Connection for Protection of Two High-Speed Data Lines

The LCDAx is designed to protect up to two high-speed data lines. The LCDAx utilizes a low capacitance compensation diode in series with, but in opposite polarity to a TVS diode in each line. The resulting capacitance is less than 5pF per line. Each line will only suppress transient events in one polarity. Therefore, to achieve protection in both positive and negative polarity, a second TVS/rectifier pair is connected in anti-parallel to the first. Pins 1, 2, 7, and 8 are used to protect one data line. Pins 3, 4, 5, and 6 are used to protect the second data line.

The device is connected as follows:

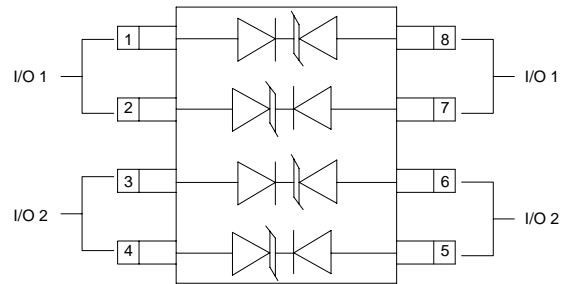
- Pins 1 & 2 are tied together and pins 7 & 8 are tied together providing the protection circuit for one I/O line. Pins 3 & 4 are tied together and pins 5 & 6 are tied together providing the protection circuit for the second I/O line. Since the device is electrically symmetrical, either side of the connected pairs may be used to protect the lines. The other side of the pair is used to make the ground connection. The ground connections should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.

Circuit Board Layout Recommendations for Suppression of ESD.

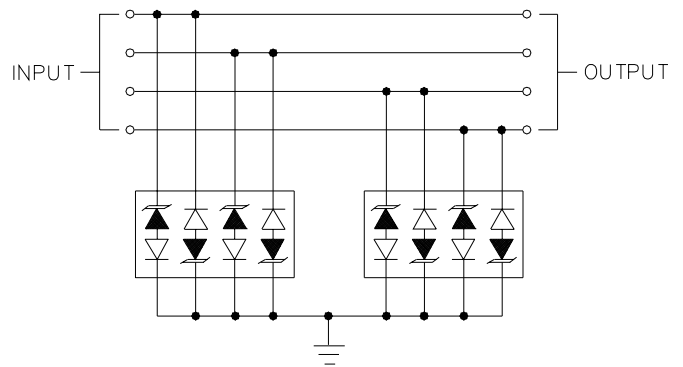
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

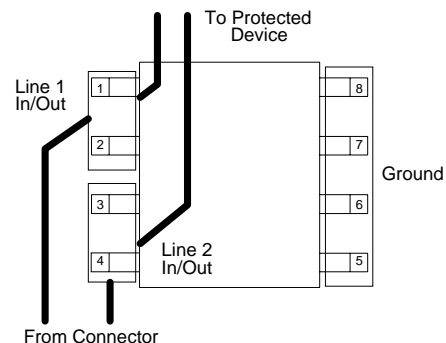
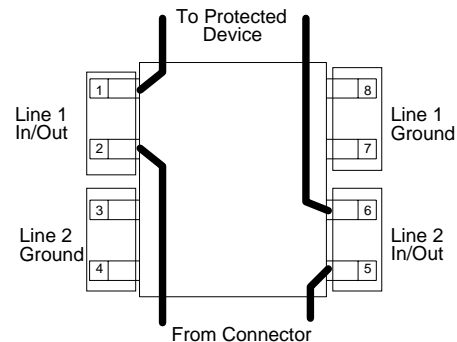
LCDA Connection Diagram



I/O Line Protection

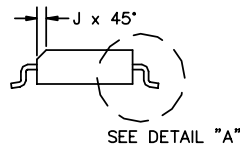
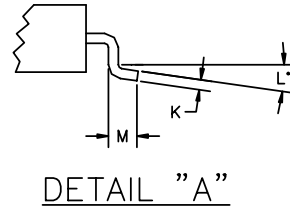
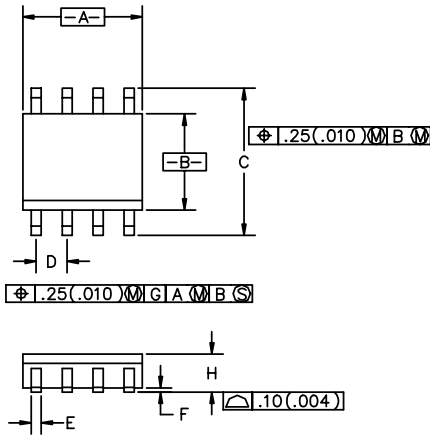


Connection Options



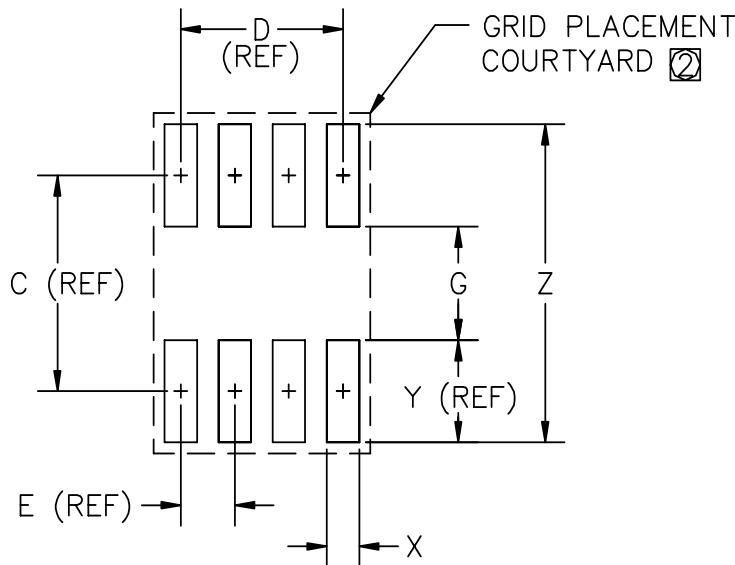
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Outline Drawing - S0-8



DIM ^N	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.188	.197	4.80	5.00	
B	.149	.158	3.80	4.00	
C	.228	.244	5.80	6.20	
D	.050	BSC	1.27	BSC	
E	.013	.020	0.33	0.51	
F	.004	.010	0.10	0.25	
H	.053	.069	1.35	1.75	
J	.011	.019	0.28	0.48	
K	.007	.010	.19	.25	
L	0°	8°	0°	8°	
M	.016	.050	0.40	1.27	

Land Pattern - S0-8



DIM ^N	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	—	.19	—	5.00	—
D	—	.15	—	3.81	—
E	—	.05	—	1.27	—
G	.10	.11	2.60	2.80	—
X	.02	.03	.60	.80	—
Y	—	.09	—	2.40	—
Z	—	.29	7.20	7.40	—

② GRID PLACEMENT COURTYARD IS 12x16 ELEMENTS (6 mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

① CONTROLLING DIMENSION: MILLIMETERS

PROTECTION PRODUCTS**Ordering Information**

Part Number	Working Voltage	Qty per Reel	Reel Size
LCDA05.TB	5V	500	7 Inch
LCDA05.TE	5V	2,500	13 Inch
LCDA12.TB	12V	500	7 Inch
LCDA12.TE	12V	2,500	13 Inch
LCDA15.TB	15V	500	7 Inch
LCDA15.TE	15V	2,500	13 Inch
LCDA24.TB	24V	500	7 Inch
LCDA24.TE	24V	2,500	13 Inch

Note:

(1) No suffix indicates tube pack.

Contact Information

Semtech Corporation
Protection Products Division
652 Mitchell Rd., Newbury Park, CA 91320
Phone: (805)498-2111 FAX (805)498-3804