EPSON

SRM2A256LLMX70/85/10

256K-Bit Static RAM

- Low Supply Current
- Access Time 70ns/85ns/100ns
- 32,768 Words×8-bit Asynchronous

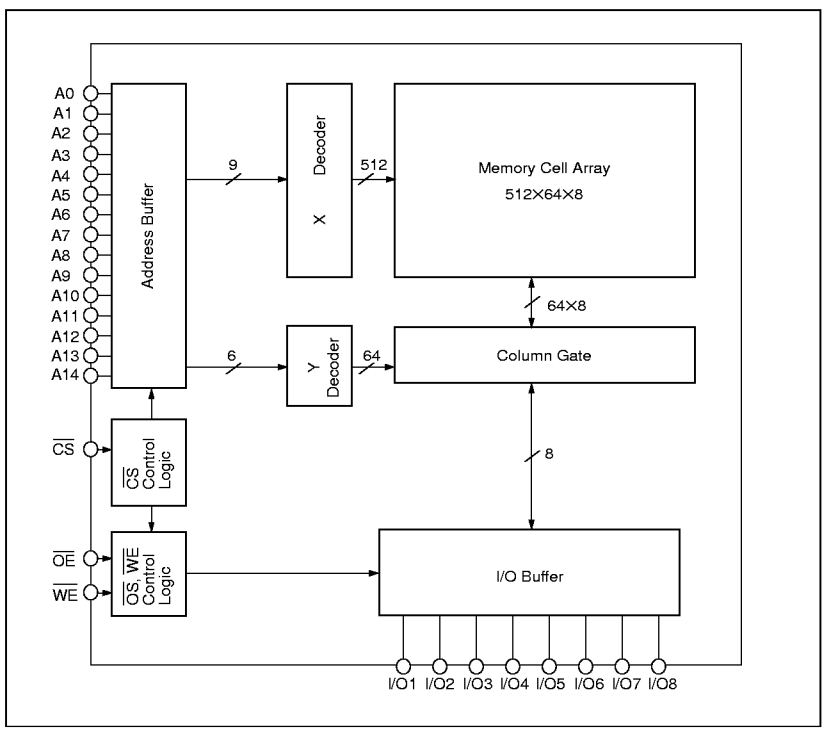
■ DESCRIPTION

The SRM2A256LLMX70/85/10 is a 32,768 wordsx8-bit asynchronous, static, random access memory fabricated using an advanced CMOS technology. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refresh circuit. Input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

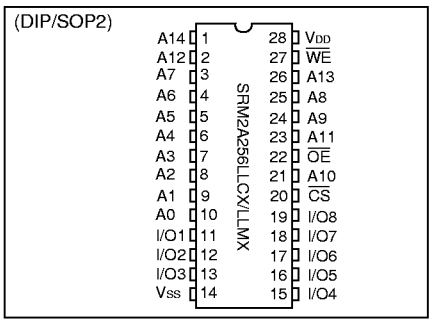
■ FEATURES

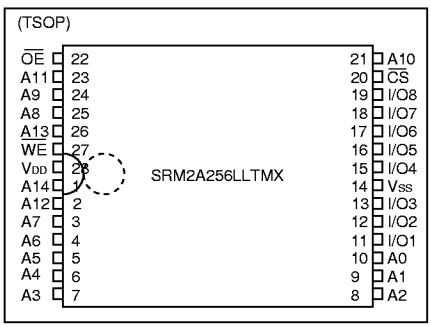
- Wide temperature range ..... –25 to 85%
- Fast access time SRM2A256LLMX70 70ns
  SRM2A256LLMX85 85ns
  SRM2A256LLMX10 100ns
- Low supply current ..... LL Version
- Completely static ..... no clock required
- Single power supply ..... 5V±10%
- TTL compatible inputs and outputs
- 3-state output
- Battery back-up operation
- Package ..... SRM2A256LLCX70/85/10 DIP-28pin (plastic)
  SRM2A256LLMX70/85/10 SOP2-28pin (plastic)
  SRM2A256LLTMX70/85/10 TSOP(I)-28pin (plastic)
  SRM2A256LLRMX70/85/10 TSOP(I)-28pin-R1 (plastic)

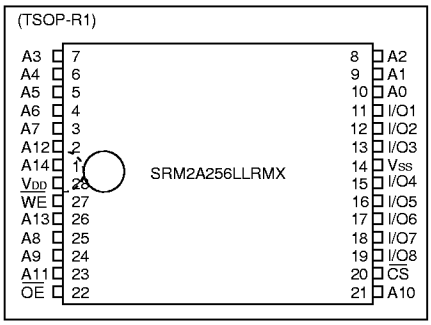
■ BLOCK DIAGRAM



■ PIN CONFIGURATION







■ PIN DESCRIPTION

A0 to A14	Address Input
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
I/01 to 08	Data Input/Output
VDD	Power Supply(+5V)
VSS	Power Supply(0V)

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.5 to 7.0	V
Input voltage	V_I	–0.5* to 7.0	V
Input/Output voltage	$V_{I/O}$	–0.5* to V_{DD}+0.3	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	–25 to 85	°C
Storage temperature	T_{stg}	–65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s(Lead only)	–

* V_I, $V_{I/O}$ (Min.)= –3V when pulse width is less or equal to 50ns

■ DC RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V, Ta=–25 to 85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
	V_{SS}		0	0	0	V
Input voltage	V_{IH}		2.2	–	V_{DD}+0.3	V
	V_{IL}		–0.3*	0	0.8	V

* V_{IL} (Min.)= –3V when pulse width is less or equal to 50ns

■ ELECTRICAL CHARACTERISTICS

● DC Electrical characyeristics

(V_{DD}=5V±10%, V_{SS}=0V, Ta=–25 to 85•C)

Parameter	Symbol	Conditions	SRM2A256LLMX70			SRM2A256LLMX85			SRM2A256LLMX10			Unit
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	Min.	Typ.	Max.	
Input leakage	V_{LI}	V_I=0 to V_{DD}	–1	–	1	–1	–	1	–1	–	1	µA
Output leakage	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH} $V_{I/O}$=0 to V_{DD}	–1	–	1	–1	–	1	–1	–	1	µA
High level output voltage	V_{OH}	I_{OH}=–1.0mA	2.4	–	–	2.4	–	–	2.4	–	–	V
Low level output voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.4	–	–	0.4	–	–	0.4	V
Standby supply current	I_{DDS}	$\overline{CS}$=V_{IH}	–	0.5	3.0	–	0.5	3.0	–	0.5	3.0	mA
	I_{DDS1}	$\overline{CS}$≥V_{DD}–0.2V	–	1	100	–	1	100	–	1	100	µA
Average operating current	I_{DDA}	V_I=V_{IL}, V_{IH} $I_{I/O}$=0mA, tcyc=Min.	–	45	70	–	45	70	–	45	70	mA
	I_{DDA1}	V_I=V_{IL}, V_{IH} $I_{I/O}$=0mA, tcyc=1µs	–	–	10	–	–	10	–	–	10	mA
Operating supply current	I_{DD0}	V_I=V_{IL}, V_{IH} $I_{I/O}$=0mA	–	–	10	–	–	10	–	–	10	mA

* : Typical values are measured at Ta=25°C and V_{DD}=5.0V

● Terminal Capacitance

(f=1MHz, Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Address Capacitance	C_{ADD}	V_{ADD}=0V	–	–	8	pF
Input Capacitance	C_I	V_I=0V	–	–	9	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	–	10	pF

● AC Electrical Characteristics

❍ Read Cycle

(V_{DD}=5V±10%, V_{SS}=0V, Ta=–25 to 85°C)

Parameter	Symbol	Conditions	SRM2A256LLMX70		SRM2A256LLMX85		SRM2A256LLMX10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	*1	70	–	85	–	100	–	ns
Address access time	t_{ACC}		–	70	–	85	–	100	ns
$\overline{CS}$ access time	t_{ACS}		–	70	–	85	–	100	ns
$\overline{OE}$ access time	t_{OE}		–	40	–	45	–	50	ns
$\overline{CS}$ output set time	t_{CLZ}	*2	10	–	10	–	10	–	ns
$\overline{CS}$ output floating	t_{CHZ}		–	30	–	30	–	35	ns
$\overline{OE}$ output set time	t_{OLZ}		0	–	0	–	0	–	ns
$\overline{OE}$ output floating	t_{OHZ}		–	30	–	30	–	35	ns
Output hold time	t_{OH}	*1	10	–	10	–	10	–	ns

❍ Write Cycle

(V_{DD}=5V±10%, V_{SS}=0V, Ta=–25 to 85°C)

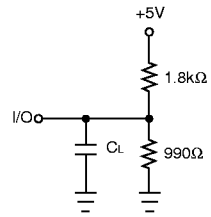
Parameter	Symbol	Conditions	SRM2A256LLMX70		SRM2A256LLMX85		SRM2A256LLMX10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	✻1	70	–	85	–	100	–	ns
Chip select time	t_{CW}		60	–	70	–	80	–	ns
Address valid to end of write	t_{AW}		60	–	70	–	80	–	ns
Address setup time	t_{AS}		0	–	0	–	0	–	ns
Write pulse width	t_{WP}		55	–	65	–	75	–	ns
Address hold time	t_{WR}		0	–	0	–	0	–	ns
Input data set time	t_{DW}		30	–	35	–	40	–	ns
Input data hold time	t_{DH}		0	–	0	–	0	–	ns
Write to Output floating	t_{WHZ}	✻2	–	30	–	30	–	35	ns
Output Active from end to wirte	t_{OW}		5	–	5	–	5	–	ns

*1 Test Conditions

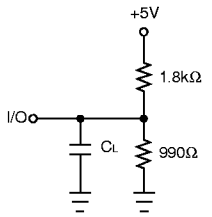
1. Input pulse level : 0.6V to 2.4V
2. t_r=t_f=5ns
3. Input and output timing reference levels : 1.5V
4. Output load : C_L=100pF

*2 Test Conditions

1. Input pulse level : 0.6V to 2.4V
2. t_r=t_f=5ns
3. Input timing reference levels : 1.5V
4. Output timing reference levels : 200mV(the level displaced from stable output voltage level)
5. Output load : C_L=5pF (Includes Jig Capacitance)



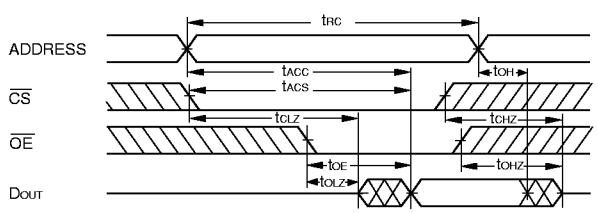
C_L=100pF (Includes Jig Capacitance)



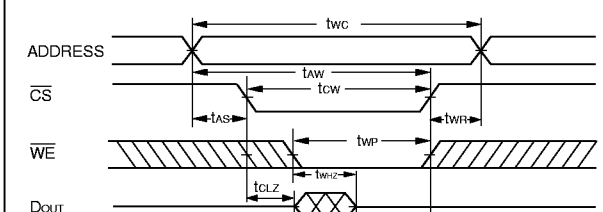
C_L=5pF (Includes Jig Capacitance)

■ Timing chart

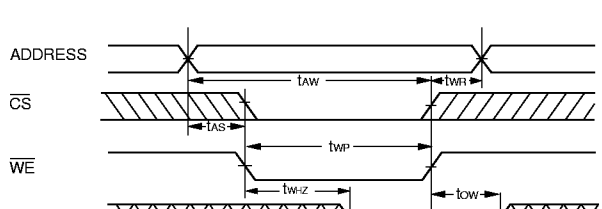
❍ Read Cycle*1



❍ Write Cycle(1) ($\overline{CS}$ Control)*2



❍ Write Cycle(2) ($\overline{WE}$ Control)*3, *4



Note :

✻1 During read cycle time, $\overline{WE}$ is to be "H" level.

✻2 During write cycle time that is controlled by $\overline{CS}$, Output Buffer is in high impedance state, whether $\overline{OE}$ level is "H" or "L"

✻3 During write cycle time that is controlled by $\overline{WE}$, Output Buffer is in high impedance state if $\overline{OE}$ is "L" level.

✻4 When I/O terminals are output mode, be careful that do not give the opposite signals to the I/O terminals.

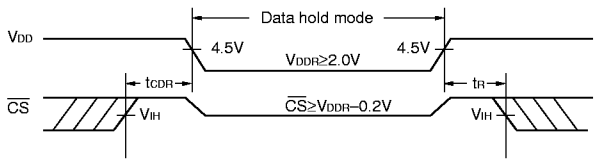
■ DARA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

(V_{SS}=0V, Ta=–25 to 85°C)

Parameter	Symbol	Conditions		SRM2A256LLMX70			SRM2A256LLMX85			SRM2A256LLMX10			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Data retention supply voltage	V_{DDR}			2.0	–	5.5	2.0	–	5.5	2.0	–	5.5	V
Data retention current	I_{DDR}	V_{DDR}=3V $\overline{CS}$≥V_{DD}–0.2V	–25 to 85°C	–	0.5	50	–	0.5	50	–	0.5	50	µA
Chip select data hold time	t_{CDR}			0	–	–	0	–	–	0	–	–	ns
Operation recovery time	t_R			5	–	–	5	–	–	5	–	–	ms

* : Typical values are measured at 25°C

Data retention timing



*When retaining data in standby mode, supply voltage can be lowered within a certain range, But read or write cycle cannot be performed while the supply voltage is low.

■ FUNCTIONS

● Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	DATA I/O	Mode	I_{DD}
H	X	X	Hi-Z	Standby	I_{DDS}, I_{DDS1}
L	X	L	D_{IN}	Write	I_{DDA}, I_{DDA1}
L	L	H	D_{OUT}	Read	I_{DDA}, I_{DDA1}
L	H	H	Hi-Z	Output disable	I_{DDA}, I_{DDA1}

X : "H" or "L"

● Read Mode

The data appear when the address is setted while holding $\overline{CS}$="L", $\overline{OE}$="L" and $\overline{WE}$ ="H". When $\overline{OE}$="H", DATA I/O terminals are in high impedance state, that makes circuit design and bus control easy.

● Write Mode

There are the following 3 ways of writing data into memory.

(1) Hold $\overline{CS}$="L" and $\overline{WE}$="L", set address.

(2) Hold $\overline{CS}$="L" then set address and give "L" pulse to $\overline{WE}$.

(3) After setting addresses, give "L" pulse to both $\overline{CS}$ and $\overline{WE}$.

In above any case data on the DATA I/O terminals are put into the SRM2A256LLMX70/85/10 when both $\overline{CS}$ and $\overline{WE}$ are in "L". Since DATA I/O terminals are high impedance when $\overline{CS}$ or $\overline{OE}$="H", bus contention between data driver and memory outputs can be avoided.

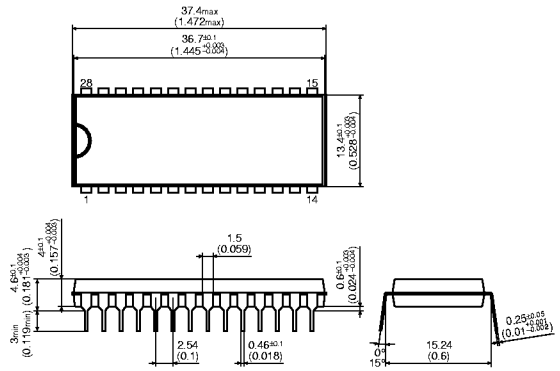
When I/O terminals are output mode, be careful that do not give the opposite signals to the I/O terminals.

● Standby Mode

When $\overline{CS}$ is "L" the SRM2A256LLMX70/85/10 become in the standby mode. In this mode, data I/O terminals are Hi-Z and all inputs of addresses, $\overline{WE}$ and data can be any "H" or "L". When $\overline{CS}$ is over than V_{DD}-0.2V, the SRM2A256LLMX70/85/10 is in the data retention battery back-up mode, in this case, there is a small current in the SRM2A256LLMX70/85/10 which flow through the high resistances of the memory cells.

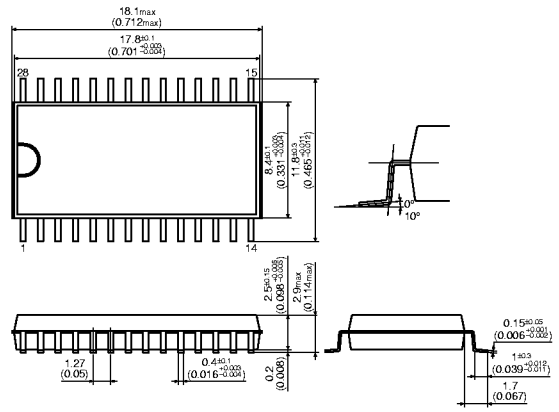
■ PACKAGE DIMENSIONS

Plastic DIP-28pin (600mil)*



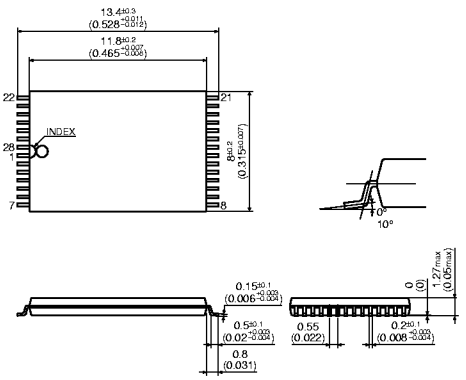
Unit : mm
(inch)

Plastic SOP2-28pin (450mil)



Unit : mm
(inch)

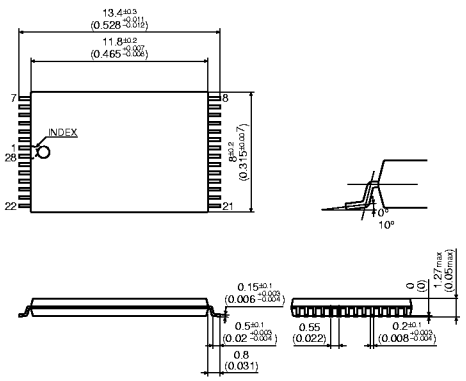
Plastic TSOP (I)-28pin*



Unit : mm
(inch)

✻ : The same characteristics as SRM2A256LLMX70/85/10.

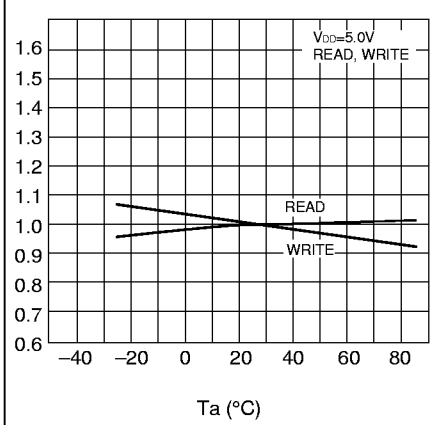
Plastic TSOP (I)-28pin-R1*



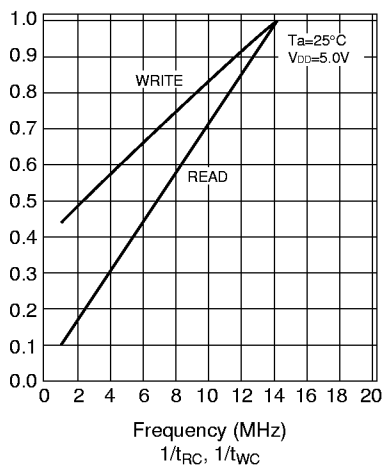
✻ : The same characteristics as SRM2A256LLMX70/85/10.

■ CARACTERISTICS CURVES

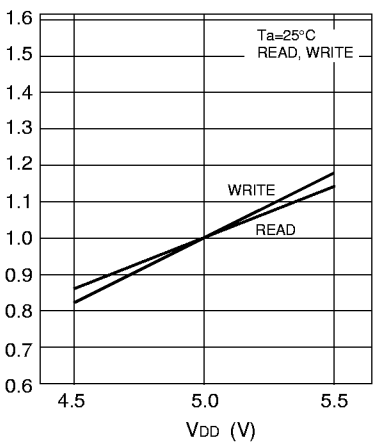
Normalized I_{DDA}–Ta



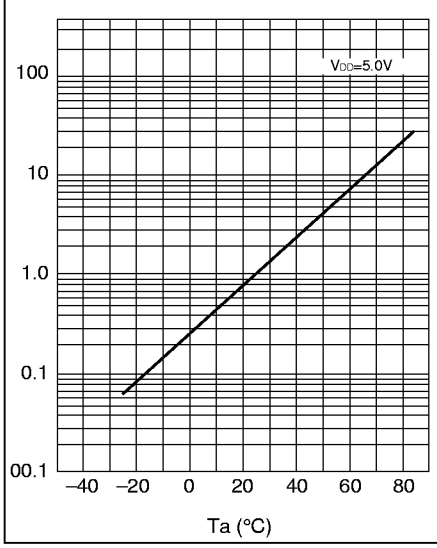
Normalized I_{DDA}–Frequency



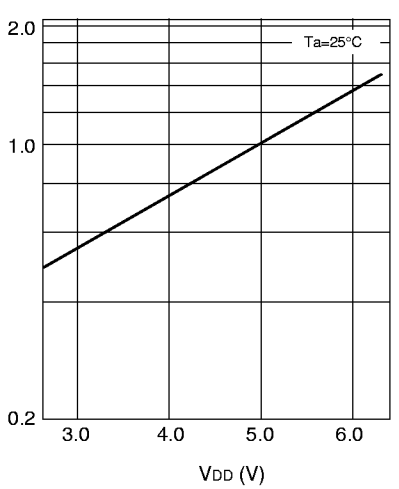
Normalized I_{DDA}–V_{DD}



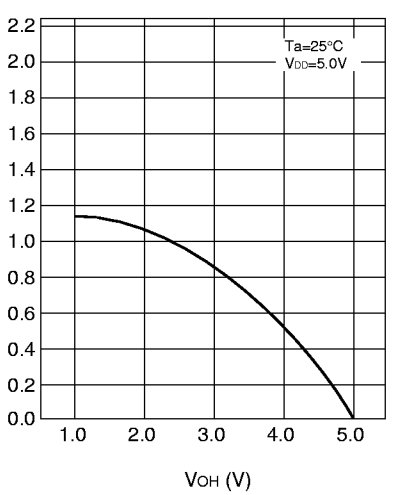
Normalized I_{DDS1}–Ta



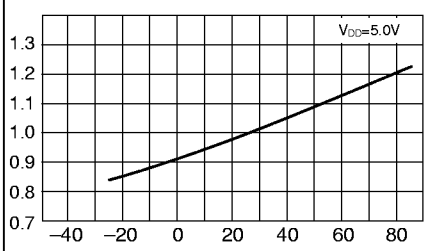
Normalized I_{DDS1}–V_{DD}



Normalized I_{OH}–V_{OH}

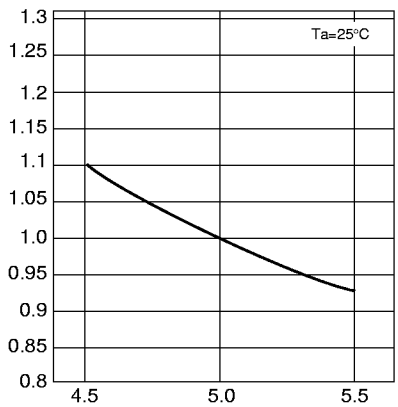


Normalized $\begin{matrix} t_{ACC} \\ t_{ACS1} \\ t_{ACS2} \end{matrix}$ –Ta



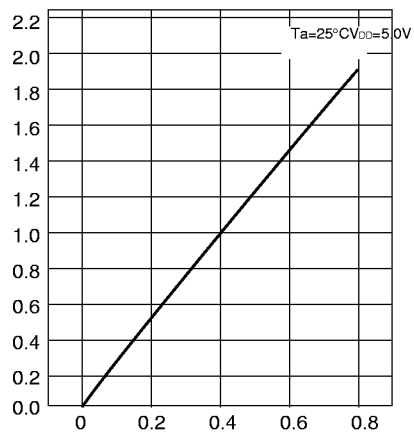
Ta (°C)

Normalized $\begin{matrix} t_{ACC} \\ t_{ACS} \end{matrix}$ –VDD



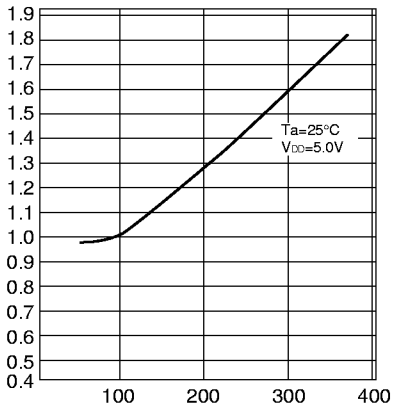
VDD (V)

Normalized IOL–VOL



VOL (V)

Normalized $\begin{matrix} t_{ACC} \\ t_{ACS} \end{matrix}$ –CL



CL (pF)