CRYSTAL OSCILLATOR

SPXO

SG-645 / SG-636 series

- Frequency range : 2.21675 MHz to 135 MHz
- Supply voltage : 2.5 V / 3.3 V / 5.0 V
- Function : Output enable(OE) or Standby($\overline{ST}$)
- External dimensions : 7.1 × 5.1 × 1.5 mm (t: Max.)···SG-645
  10.5 × 5.8 × 2.7 mm (t: Max.)···SG-636

RoHS Compliant

Product Number (please contact us)
SG-645 : Q33645xx1xxxx00
SG-636 : Q33636xx1xxxx00

Actual size

SG-645 series

SG-636 series

Specifications (characteristics)

Item	Symbol	Specifications			Conditions / Remarks
		SG-636 PTF	SG-636 PCE SG-636 SCE	SG-636 PDE	
Output frequency range	f_0	2.21675 MHz to 41.000 MHz	2.21675 MHz to 40.000 MHz	2.21675 MHz to 40.000 MHz	
Supply voltage	V_{CC}	5.0 V ±0.5 V	3.3 V ±0.3 V	2.5 V ±0.25 V	
Storage temperature	T_stg	-55 °C to +100 °C			Store as bare product.
Operating temperature	T_use	-20 °C to +70 °C			
Frequency tolerance	f_tol	C: ±100 × 10^{-6}			-20 °C to +70 °C
Current consumption	I_{CC}	17 mA Max.	9 mA Max.	5 mA Max.	No load condition
Disable current	I_dis	10 mA Max.	5 mA Max.	3 mA Max.	OE=GND
Stand-by current	I_std	—	2 µA Max.	—	$\overline{ST}$ =GND(SCE)
Symmetry	SYM	40 % to 60 %	45 % to 55 %		CMOS load:50 % V_{CC} level
		45 % to 55 %	—		TTL load: 1.4 V level
Output voltage	V_{OH}	V_{CC}-0.4 V Min.			I_{OH}=-8 mA(PTF) / -4 mA(SCE,PCE) / -3.2 mA(PDE)
	V_{OL}	0.4 V Max.			I_{OL}=16 mA(PTF) / 4 mA(SCE,PCE) / 3.2 mA(PDE)
Output load condition (TTL)	L_TTL	10 TTL Max.	—		L_CMOS ≤ 15 pF
Output load condition (CMOS)	L_CMOS	50 pF Max.	30 pF Max.	15 pF Max.	
Input voltage	V_{IH}	2.0 V Min.	80 % V_{CC} Min.		OE Terminal or $\overline{ST}$ Terminal (SCE)
	V_{IL}	0.8 V Max.	20 % V_{CC} Max.		
Rise time / Fall time	t_r / t_f	7 ns Max.	5 ns Max.		CMOS load:20 % V_{CC} to 80 % V_{CC} level
		5 ns Max.	—		TTL load:0.4 V to 2.4 V level
Start-up time	t_str	4 ms Max.	4 ms Max.		Time at minimum supply voltage to be 0 s
Frequency aging	f_aging	±5 × 10^{-6} / year Max.			+25 °C, V_{CC}=5.0 V/3.3 V/2.5 V, First year

Specifications (characteristics)

Item	Symbol	Specifications			Conditions / Remarks
		SG-636 PTG	SG-636 PHG	SG-636 PCG SG-636 SCG	
Output frequency range	f_0	2.21675 MHz to 33.000 MHz *1			
Supply voltage	V_{CC}	4.5 V to 5.5 V		2.7 V to 3.6 V	
Storage temperature	T_stg	-55 °C to +100 °C			Store as bare product.
Operating temperature	T_use	-20 °C to +70 °C			
Frequency tolerance	f_tol	B: ±50 × 10^{-6} C: ±100 × 10^{-6}			-20 °C to +70 °C
Current consumption	I_{CC}	25 mA Max.		12 mA Max.	No load condition
Disable curren	I_dis	20 mA Max.		10 mA Max.	OE=GND (PTG,PHG,PCG)
Stand-by current	I_std	—		50 µA Max.	$\overline{ST}$ =GND (SCG)
Symmetry	SYM	—	45 % to 55 %		50 % V_{CC} level, L_CMOS=25 pF
		40 % to 60 %	—		1.4 V level, L_CMOS=25 pF
Output voltage	V_{OH}	2.4 V Min.	—	V_{CC}-0.4 V Min.	I_{OH}=-8 mA
		—	V_{CC}-0.4 V Min.	—	I_{OH}=-16 mA
	V_{OL}	—		0.4 V Max.	I_{OL}=8 mA
		0.4 V Max.		—	I_{OL}=16 mA
Output load condition	L_CMOS	25 pF Max.			
Input voltage	V_{IH}	2.0 V Min.		70 % V_{CC} Min.	OE Terminal or $\overline{ST}$ Terminal
	V_{IL}	0.8 V Max.		20 % V_{CC} Max.	
Rise time / Fall time	t_r / t_f	—	3.4 ns Max.	4 ns Max.	20 % V_{CC} to 80 % V_{CC} level, L_CMOS ≤ 25 pF
		2.4 ns Max.	—		TTL load:0.4 V to 2.4 V level, L_CMOS ≤ 25 pF
Start-up time	t_str	12 ms Max.			t=0 at 90 % V_{CC}
Frequency aging	f_aging	±5 × 10^{-6} / year Max.			+25 °C, V_{CC}=5.0 V/ 3.3 V, First year

*1 4.1250 MHz < fo < 4.4336 MHz, 8.2500 MHz < fo < 8.8672 MHz, 16.500 MHz < fo < 17.7344 MHz : Unavailable

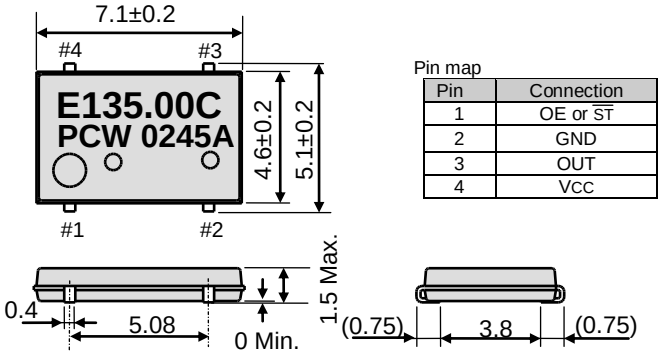
Specifications (characteristics)

Item	Symbol	Specifications			Conditions / Remarks
		SG-636 PTW / STW SG-645 PTW / STW	SG-636 PHW / SHW SG-645 PHW / SHW	SG-636 PCW / SCW SG-645 PCW / SCW	
Output frequency range	f_0	32.001 MHz to 135.000 MHz			
Supply voltage	Vcc	5.0 V ±0.5 V		3.3 V ±0.3 V	
Storage temperature	T_stg	SG-636P**:-55 °C to +100 °C / SG-645P**:-55 °C to +125 °C			Store as bare product.
Operating temperature	T_use	-20 °C to +70 °C			
		—		-40 °C to +85 °C	SG-645PCW / SCW Only
Frequency tolerance	f_tol	B: ±50 × 10^{-6} C: ±100 × 10^{-6}			-20 °C to +70 °C *1
		—		M: ±100 × 10^{-6}	-40 °C to +85 °C : SG-645PCW / SCW Only
Current consumption	Icc	45 mA Max.		28 mA Max.	No load condition(Max. frequency range)
Disable current	I_dis	30 mA Max.		16 mA Max.	OE=GND (PTW,PHW,PCW)
Stand-by current	I_std	50 µA Max.			$\overline{ST}$ =GND (STW,SHW,SCW)
Symmetry	SYM	—	40 % to 60 %		50 % Vcc level, L_CMOS=Max.
		40 % to 60 %	—		1.4 V level, L_CMOS=Max.
Output voltage	VOH	Vcc-0.4 V Min.			IOH=-16 mA(PTW , STW , PHW , SHW) /-8 mA(PCW , SCW)
	VOL	0.4 V Max.			IOL= 16 mA(PTW , STW , PHW , SHW) / 8 mA(PCW , SCW)
Output load condition (TTL)	L_TTL	5 TTL Max.	—	—	fo≤ 90 MHz, Max.Supply voltage.
Output load condition (CMOS)	L_CMOS	15 pF Max.			Max.frequency, Max.Supply voltage.
Input voltage	VIH	2.0 V Min.		70 % Vcc Min.	OE Terminal or $\overline{ST}$ Terminal
	VIL	0.8 V Max.		20 % Vcc Max.	
Rise time / Fall time	tr / tf	—	4 ns Max.		20 % Vcc to 80 % Vcc level, L_CMOS ≤ Max.
		4 ns Max.	—	—	0.4 V to 2.4 V level
Start-up time	t_str	10 ms Max.			Time at minimum supply voltage to be 0 s
Frequency aging	f_aging	±5 × 10^{-6} / year Max.			+25 °C, Vcc=5.0 V / 3.3 V, First year

*1 SG-636 series "C" tolerance : 40 MHz<fo≤135 MHz

External dimensions (Unit:mm)

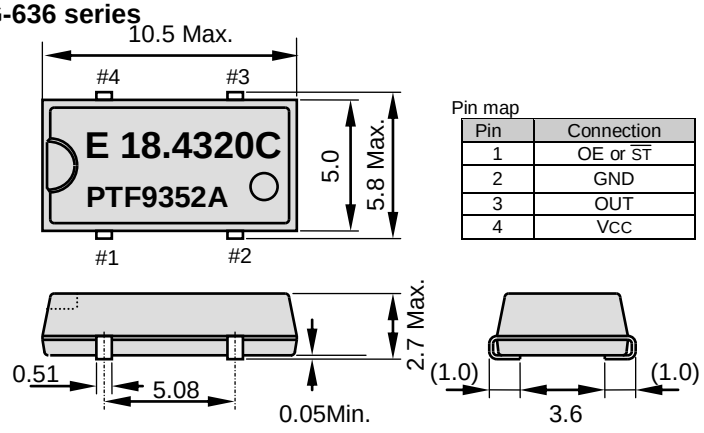
SG-645 series



Pin map

Pin	Connection
1	OE or $\overline{ST}$
2	GND
3	OUT
4	Vcc

SG-636 series



Pin map

Pin	Connection
1	OE or $\overline{ST}$
2	GND
3	OUT
4	Vcc

Metal may be exposed on the top or bottom of this product.
This will not affect any quality, reliability or electrical spec.

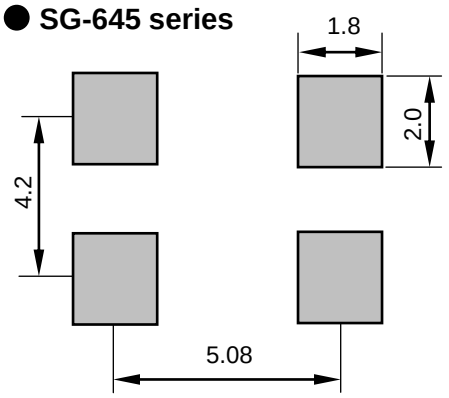
Note.
OE pin (PTF,PCE,PDE,PTW,PHW,PCW,PTG,PHG,PCG)
OE pin = "H" or "open" : Specified frequency output.
OE pin = "L" : Output is high impedance.

$\overline{ST}$ pin (STW, SHW, SCW,SCG)
$\overline{ST}$ pin = "H" or "open" : Specified frequency output.
$\overline{ST}$ pin = "L" : Output is low level (weak pull - down),oscillation stops.

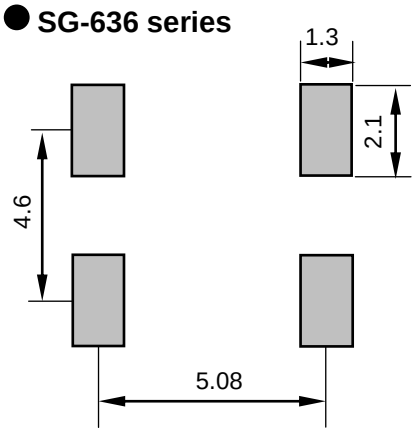
$\overline{ST}$ pin (SCE)
$\overline{ST}$ pin = "H" or "open" : Specified frequency output.
$\overline{ST}$ pin = "L" : Output is low level ,oscillation stops.

Footprint (Recommended) (Unit:mm)

SG-645 series



SG-636 series



To maintain stable operation, provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).