



# Microcomputer Components

8-bit CMOS Microcontroller

## C513AO

Data Sheet 02.00

<http://www.infineon.com/>

<b>C513AO Data Sheet</b>		
<b>Revision History :</b>		<b>Current Version: 02.00</b>
Previous Releases:		(Original Version)

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#### **Edition 02.00**

**Published by Infineon Technologies AG,  
St.-Martin-Strasse 53,  
D-81541 München**

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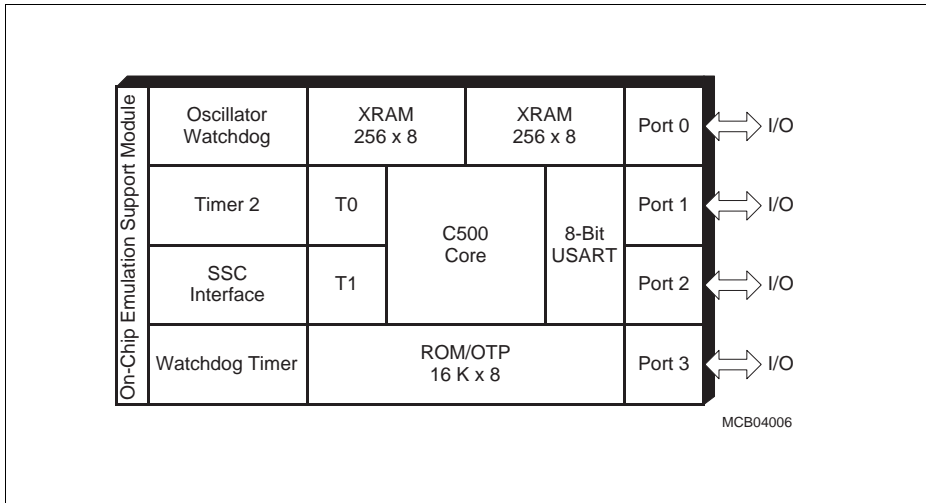
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## Advance Information

- Full upward compatibility with standard 8051 microcontroller
- Up to 16 MHz external operating frequency
  - 750 ns instruction cycle at 16 MHz operation
- On-chip program memory
  - C513AO-2R: 16 Kbytes ROM (with optional ROM protection)
  - C513AO-2E: 16 Kbytes OTP
  - C513AO-L: version without on-chip program memory (ROMless)
- Up to 64K byte external data memory
- 256 × 8 RAM
- 256 × 8 XRAM
- Four 8-bit digital I/O ports
- Three 16-bit timers/counters (Timer 2 with Up/Down and 16-bit auto-reload features)
- Full duplex serial interface (USART)
- Synchronous Serial Channel (SSC)
- Seven interrupt sources with two priority levels
- On-chip emulation support logic (Enhanced Hooks Emulation Technology™)

(further features are on next page)



**Figure 1**  
**C513AO Functional Units**

Features (continued):

- Programmable 15-bit Watchdog Timer
- Oscillator Watchdog
- Fast Power On Reset
- Power Saving Modes
  - Slow-down mode
  - Idle mode
  - Software power-down mode with optional wake up capability through pin P3.2/ $\overline{\text{INT0}}$
- Available in P-DIP40-2, P-LCC-44-1 and P-MQFP-44-2 packages
- Fully pin-compatible with C501, C504, C505C, C505CA and C511/C513-devices.
- Temperature ranges: SAB-C513AO  $T_A$ : 0 to 70 °C  
SAF-C513AO  $T_A$ : – 40 to 85 °C

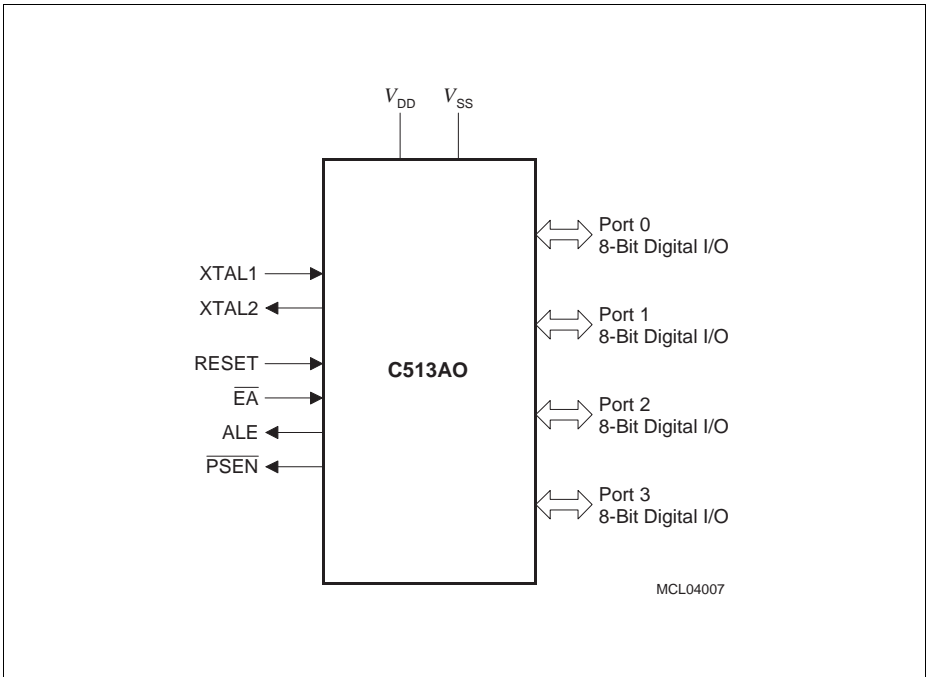
### Ordering Information

The ordering code for Siemens microcontrollers provides an exact reference to the required product. This ordering code identifies:

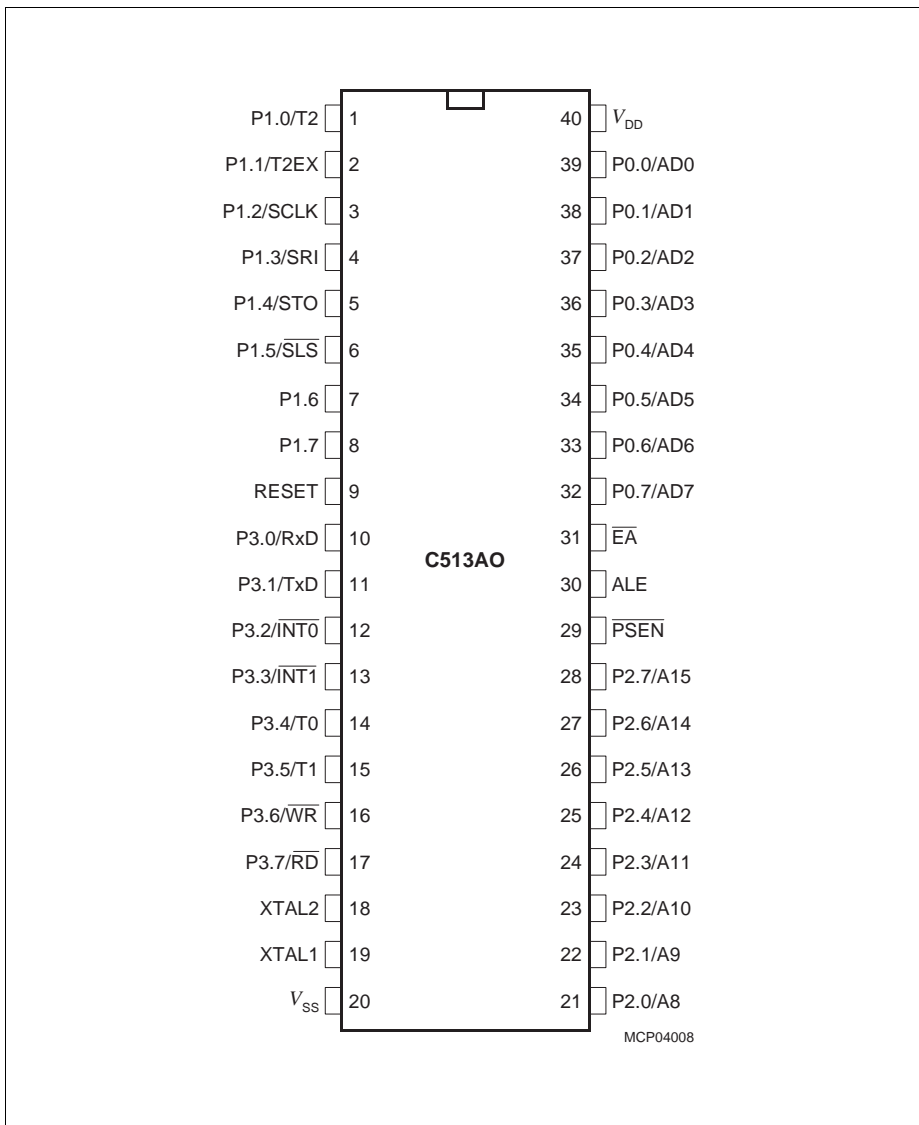
- the derivative itself, i.e. its function set
- the specified temperature range
- the package and the type of delivery

For the available ordering codes for the C513AO please refer to the “**Product Information Microcontrollers**”, which summarizes all available microcontroller variants.

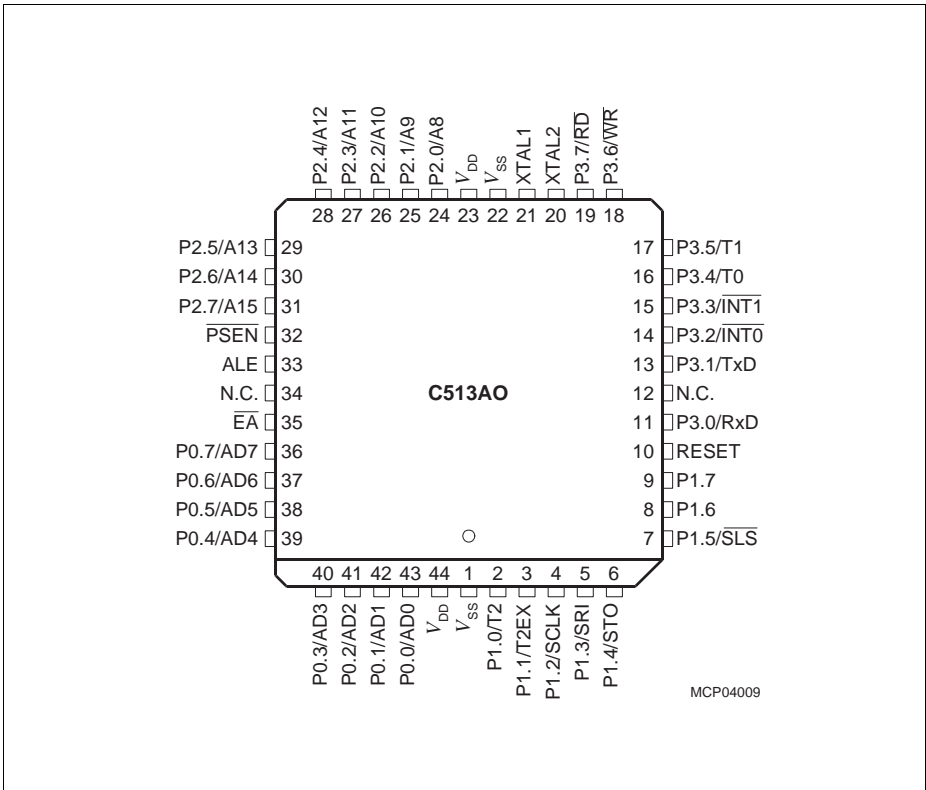
*Note: The ordering codes for the Mask-ROM versions are defined for each product after the verification of the respective ROM code.*



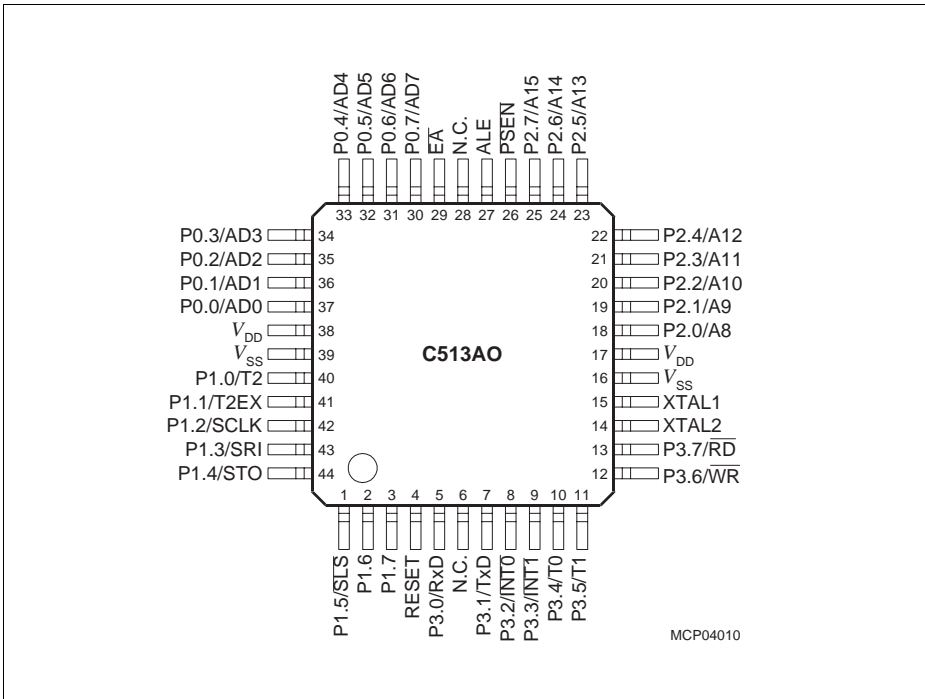
**Figure 2**  
**Logic Symbol**



**Figure 3**  
**P-DIP-40-2 Package Pin Configuration (top view)**



**Figure 4**  
**P-LCC-44-1 Package Pin Configuration (top view)**



**Figure 5**  
**P-MQFP-44-2 Package Pin Configuration (top view)**



**Table 1**  
**Pin Definitions and Functions**

Symbol	Pin Number			I/O )	Function
	P- DIP -40	P-LCC- 44	P-MQFP- 44		
P1.7- P1.0	8-1	9-2	3-1, 44-40	I/O	<p>Port 1</p> <p>Port 1 is an 8-bit quasi-bidirectional port with internal pull-up arrangement. Port 1 pins that have "1s" written to them are pulled high by the internal pull-up transistors and in that state can be used as inputs. As inputs, Port 1 pins being externally pulled low will source current (<math>I_{IL}</math>, in the DC characteristics) because of the internal pull-up transistors. The output latch corresponding to a secondary function must be programmed to 1 for that function to operate.</p> <p>For the outputs of the Synchronous Serial Channel (SSC), SCLK and STO, special circuitry is implemented providing true push-pull capability. The STO output, in addition, will have true tristate capability. When used for SSC inputs, the pull-up transistors will be switched off and the inputs float (high ohm inputs).</p> <p>The secondary functions are assigned to the pins of Port 1 as follows:</p>
	1	2	40		P1.0 / T2      Input to Counter 2
	2	3	41		P1.1 / T2EX    Capture/reload trigger of Timer 2
	3	4	42		Up-Down count
	4	5	43		P1.2 / SCLK    SSC Master Clock Output
	5	6	44		SSC Slave Clock Input
	6	7	1		P1.3 / SRI      SSC Receive Input
					P1.4 / STO      SSC Transmit Output
					P1.5 / $\overline{SLS}$ Slave Select Input

\*) I = Input  
 O = Output

**Table 1**  
**Pin Definitions and Functions (cont'd)**

Symbol	Pin Number			I/O )	Function																
	P- DIP -40	P-LCC- 44	P-MQFP- 44																		
P3.0- P.3.7	10-17	11, 13-19	5, 7-13	I/O	<p><b>Port 3</b></p> <p>Port 3 is an 8-bit quasi-bidirectional port with internal pull-up arrangement. Port 3 pins that have "1"s written to them are pulled high by the internal pull-up transistors and in that state can be used as inputs. As inputs, Port 3 pins being externally pulled low will source current (<math>I_{IL}</math>, in the DC characteristics) because of the internal pull-up transistors. The output latch corresponding to a secondary function must be programmed to a "1" for that function to operate (except for TxD and WR).</p> <p>The secondary functions are assigned to the pins of Port 3 as follows:</p> <table border="0"> <tr> <td>P3.0 / RxD</td> <td>Receiver data input (asynch.) or data input/output (synch.) of serial interface</td> </tr> <tr> <td>P3.1 / TxD</td> <td>Transmitter data output (asynch.) or clock output (synch.) of serial interface</td> </tr> <tr> <td>P3.2 / <math>\overline{\text{INT0}}</math></td> <td>External Interrupt 0 input / Timer 0 gate control input</td> </tr> <tr> <td>P3.3 / <math>\overline{\text{INT1}}</math></td> <td>External Interrupt 1 input / Timer 1 gate control input</td> </tr> <tr> <td>P3.4 / T0</td> <td>Timer 0 counter input</td> </tr> <tr> <td>P3.5 / T1</td> <td>Timer 1 counter input</td> </tr> <tr> <td>P3.6 / <math>\overline{\text{WR}}</math></td> <td><math>\overline{\text{WR}}</math> control output; latches the data byte from Port 0 into the external data memory</td> </tr> <tr> <td>P3.7 / <math>\overline{\text{RD}}</math></td> <td><math>\overline{\text{RD}}</math> control output; enables the external data memory to Port 0</td> </tr> </table>	P3.0 / RxD	Receiver data input (asynch.) or data input/output (synch.) of serial interface	P3.1 / TxD	Transmitter data output (asynch.) or clock output (synch.) of serial interface	P3.2 / $\overline{\text{INT0}}$	External Interrupt 0 input / Timer 0 gate control input	P3.3 / $\overline{\text{INT1}}$	External Interrupt 1 input / Timer 1 gate control input	P3.4 / T0	Timer 0 counter input	P3.5 / T1	Timer 1 counter input	P3.6 / $\overline{\text{WR}}$	$\overline{\text{WR}}$ control output; latches the data byte from Port 0 into the external data memory	P3.7 / $\overline{\text{RD}}$	$\overline{\text{RD}}$ control output; enables the external data memory to Port 0
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P3.7 / $\overline{\text{RD}}$	$\overline{\text{RD}}$ control output; enables the external data memory to Port 0																				
RESET	9	10	4	I	<p><b>RESET</b></p> <p>A high level on this pin for the duration of two machine cycles while the oscillator is running resets the device. An internal diffused resistor to <math>V_{SS}</math> permits power-on reset using only an external capacitor to <math>V_{DD}</math>.</p>																

\*) I = Input  
 O = Output

**Table 1**  
**Pin Definitions and Functions (cont'd)**

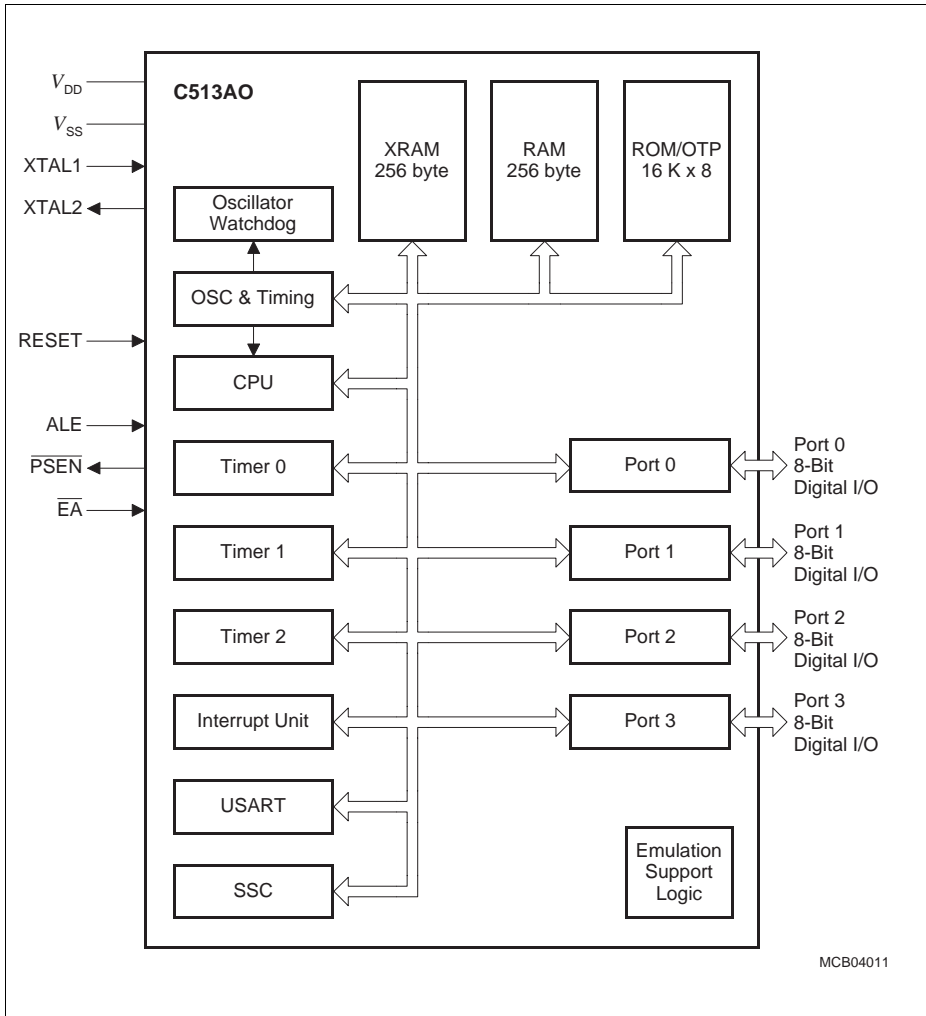
Symbol	Pin Number			I/O )*)	Function
	P- DIP -40	P-LCC- 44	P-MQFP- 44		
XTAL2	18	20	14	O	<b>XTAL2</b> Output of the inverting oscillator amplifier.
XTAL1	19	21	15	I	<b>XTAL1</b> Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.
P2.0- P2.7	21-28	24-31	18-25	I/O	<b>Port 2</b> Port 2 is an 8-bit quasi-bidirectional I/O port with internal pull-up arrangement. Port 2 pins that have "1s" written to them are pulled high by the internal pull-up transistors, and in that state can be used as inputs. As inputs, Port 2 pins being externally pulled low will source current ( $I_{IL}$ , in the DC characteristics) because of the internal pullup transistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup transistors when issuing "1"s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), Port 2 issues the contents of the P2 Special Function Register and uses only the internal pull-up transistors.
PSEN	29	32	26	O	<b>Program Store Enable</b> This is a control signal that enables output of the external program memory to the bus during external fetch operations. It is activated every three oscillator periods except during external data memory accesses. It remains high during internal program execution. This pin should not be driven during reset operation.

\*) I = Input  
O = Output

**Table 1**  
**Pin Definitions and Functions (cont'd)**

Symbol	Pin Number			I/O )	Function
	P-DIP -40	P-LCC- 44	P-MQFP- 44		
ALE	30	33	27	O	<b>Address Latch Enable</b> This output is used for latching the low-byte of the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access. When instructions are executed from internal program memory ( $\overline{EA} = 1$ ) the ALE generation can be disabled by bit EALE in SFR SYSCON. This pin should not be driven during reset operation.
$\overline{EA}$	31	35	29	I	<b>External Access Enable</b> When held at high level, instructions are fetched from the internal program memory when the PC is less than 4000 <sub>H</sub> . When held at low level, the C513AO fetches all instructions from external program memory. This pin should not be driven during reset operation. <b>Note:</b> For the C513AO-L this pin must be tied low.
P0.0- P0.7	32-39	43-36	37-30	I/O	<b>Port 0</b> Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have "1s" written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application, it uses strong internal pull-up transistors when issuing 1s. External pull-up resistors are required during program verification.
$V_{SS}$	20	22, 1	16, 39	–	<b>Ground</b> (0 V)
$V_{DD}$	40	44, 23	38, 17	–	<b>Power Supply</b> (+ 5 V)
N.C.	–	12, 34	6, 28	–	<b>No Connection.</b> These pins should not be connected.

\*) I = Input  
 O = Output



**Figure 6**  
**Block Diagram of the C513AO**

**CPU**

The C513AO is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 16-MHz crystal, 58% of the instructions execute in 750 ns.

**Special Function Register PSW (Address D0<sub>H</sub>)**
**Reset Value: 00<sub>H</sub>**

	MSB							LSB	
	D7 <sub>H</sub>	D6 <sub>H</sub>	D5 <sub>H</sub>	D4 <sub>H</sub>	D3 <sub>H</sub>	D2 <sub>H</sub>	D1 <sub>H</sub>	D0 <sub>H</sub>	
D0 <sub>H</sub>	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

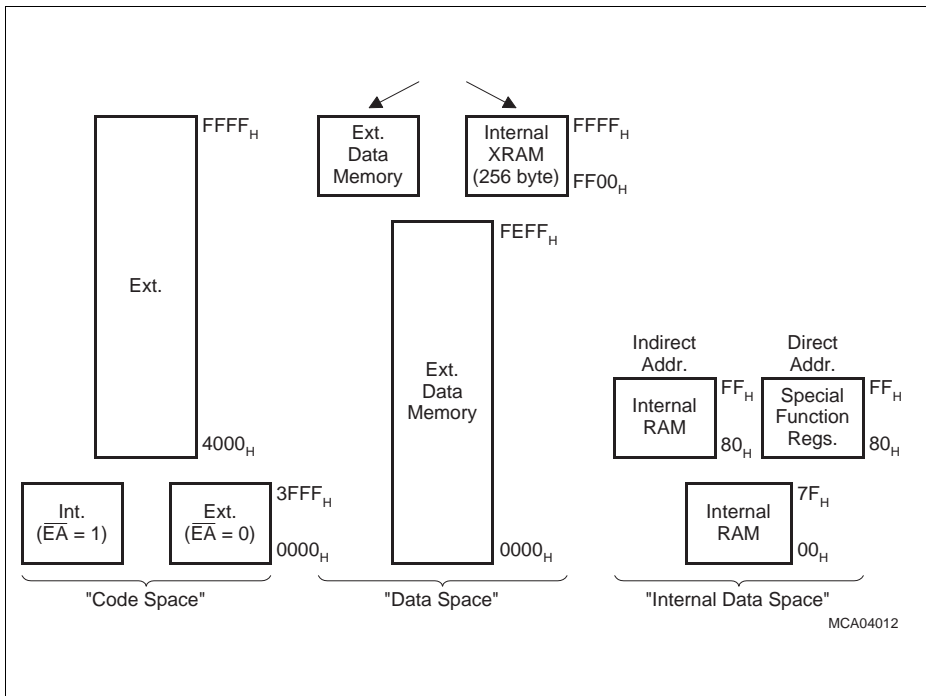
Bit	Function															
CY	<b>Carry Flag</b> Used by arithmetic instruction.															
AC	<b>Auxiliary Carry Flag</b> Used by instructions which execute BCD operations.															
F0	<b>General Purpose Flag 0</b>															
RS1 RS0	<b>Register bank Select control bits</b> These bits are used to select one of the four register banks.															
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">RS1</th> <th style="width: 15%;">RS0</th> <th style="width: 70%;">Function</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td>Bank 0 selected, data address 00<sub>H</sub>-07<sub>H</sub></td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td>Bank 1 selected, data address 08<sub>H</sub>-0F<sub>H</sub></td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td>Bank 2 selected, data address 10<sub>H</sub>-17<sub>H</sub></td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td>Bank 3 selected, data address 18<sub>H</sub>-1F<sub>H</sub></td> </tr> </tbody> </table>	RS1	RS0	Function	0	0	Bank 0 selected, data address 00 <sub>H</sub> -07 <sub>H</sub>	0	1	Bank 1 selected, data address 08 <sub>H</sub> -0F <sub>H</sub>	1	0	Bank 2 selected, data address 10 <sub>H</sub> -17 <sub>H</sub>	1	1	Bank 3 selected, data address 18 <sub>H</sub> -1F <sub>H</sub>
RS1	RS0	Function														
0	0	Bank 0 selected, data address 00 <sub>H</sub> -07 <sub>H</sub>														
0	1	Bank 1 selected, data address 08 <sub>H</sub> -0F <sub>H</sub>														
1	0	Bank 2 selected, data address 10 <sub>H</sub> -17 <sub>H</sub>														
1	1	Bank 3 selected, data address 18 <sub>H</sub> -1F <sub>H</sub>														
OV	<b>Overflow Flag</b> Used by arithmetic instruction.															
F1	<b>General Purpose Flag 1</b>															
P	<b>Parity Flag</b> Set/cleared by hardware after each instruction to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.															

### Memory Organization

The C513AO CPU manipulates operands in the following five address spaces:

- Up to 64 Kbytes of program memory (up to 16 KB on-chip program memory for the C513AO-2R/2E)
- Up to 64 Kbytes of external data memory
- 256 bytes of internal data memory
- 256 bytes of internal XRAM data memory
- One 128-byte special function register area

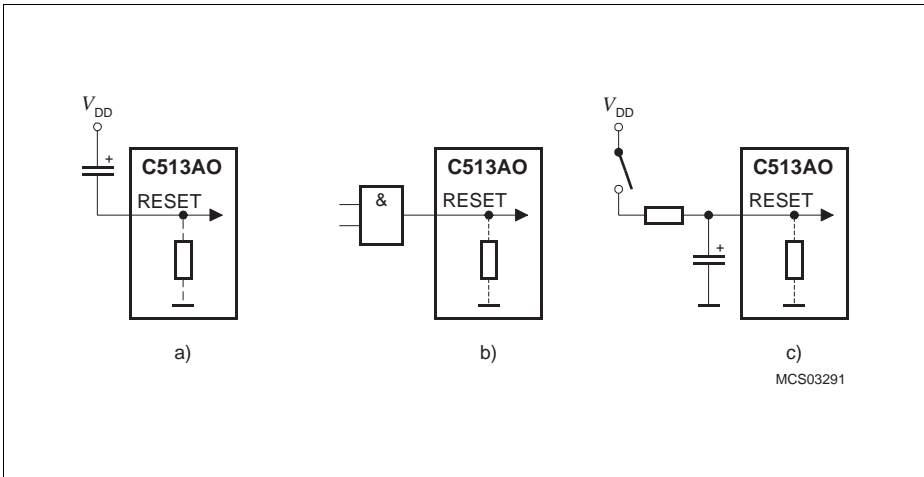
Figure 7 illustrates the memory address spaces of the C513AO.



**Figure 7**  
**C513AO Memory Map**

**Reset and System Clock**

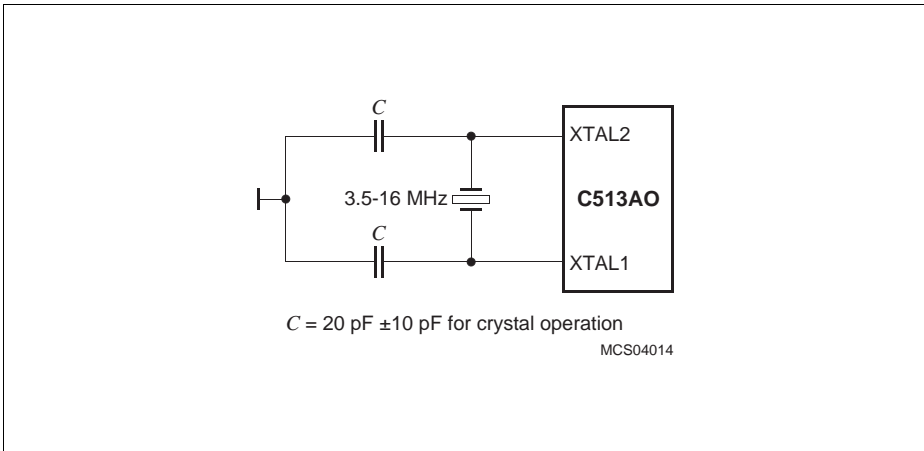
The reset input is an active high input. An internal Schmitt-trigger is used at the input for noise rejection. Since the reset is synchronized internally, the RESET pin must be held high for at least two machine cycles (24 oscillator periods) while the oscillator is running. With the oscillator running, the internal reset is executed during the second machine cycle and is repeated every cycle until RESET goes low again. **Figure 8** shows the possible reset circuitries.



**Figure 8**  
**Reset Circuitries**

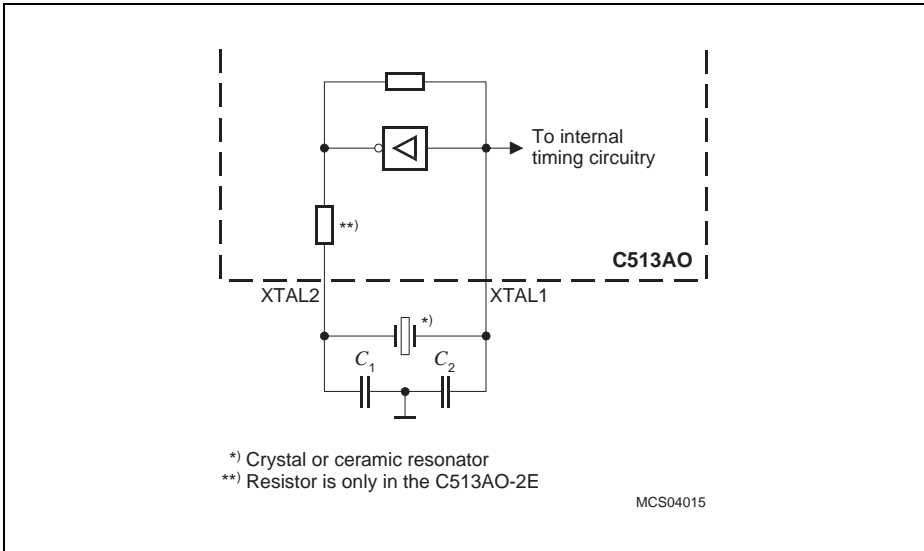


Figure 9 shows the recommended oscillator circuitries for crystal and external clock operation.



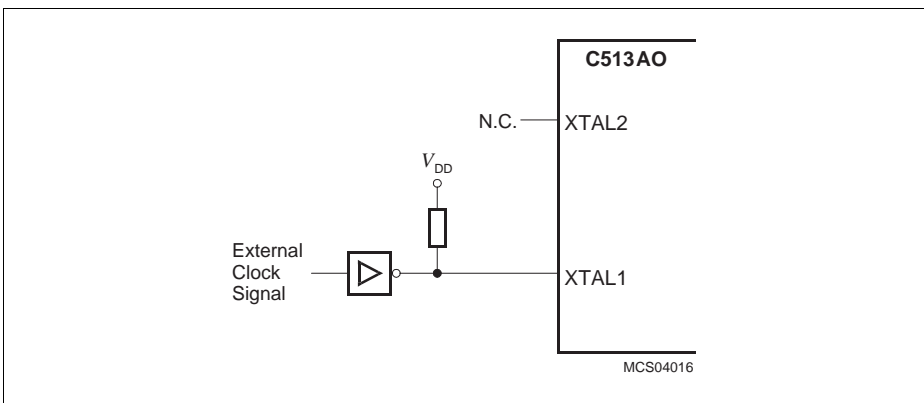
**Figure 9**  
**Recommended Oscillator Circuitry**

In this application, the on-chip oscillator is used as a crystal-controlled, positive-reactance oscillator (a more detailed schematic is given in **Figure 10**). It is operated in its fundamental response mode as an inductive reactor in parallel resonance with a capacitor external to the chip. The crystal specifications and capacitances are non-critical. In this circuit, 20 pF can be used as single capacitance at any frequency together with a good quality crystal. A ceramic resonator can be used in place of the crystal in cost-critical applications. If a ceramic resonator is used, the two capacitors normally will have different values, dependent on the oscillator frequency. We recommend consulting the manufacturer of the ceramic resonator for value specifications of these capacitors.



**Figure 10**  
**On-Chip Oscillator Circuitry**

To drive the C513AO with an external clock source, the external clock signal must be applied to XTAL1, as shown in **Figure 11**. XTAL2 must be left unconnected. A pull-up resistor is suggested to increase the noise margin, but is optional if  $V_{OH}$  of the driving gate corresponds to the  $V_{IH2}$  specification of XTAL1.



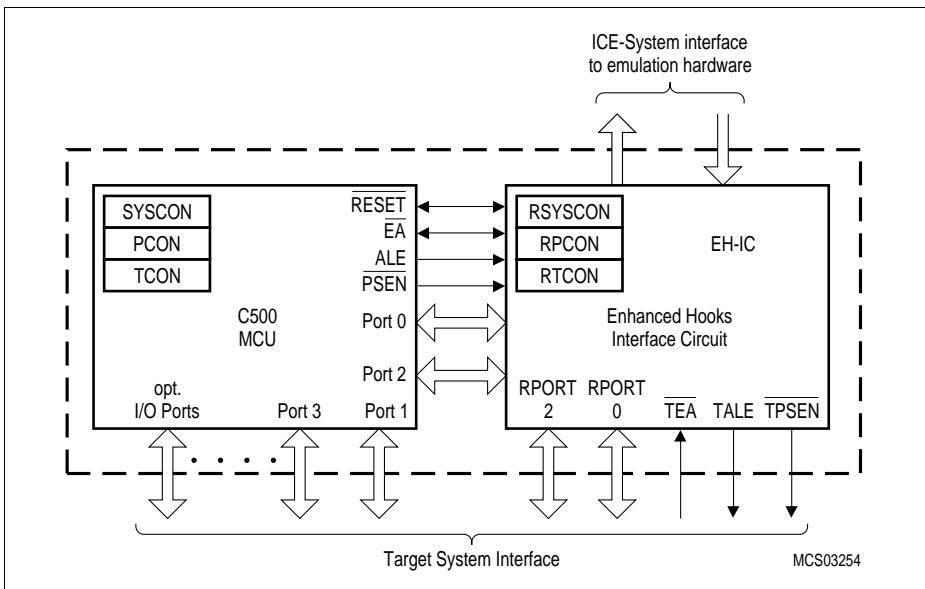
**Figure 11**  
**External Clock Source**

**Enhanced Hooks Emulation Concept**

The Enhanced Hooks Emulation Concept of the C500 microcontroller family is a new, innovative way to control the execution of C500 MCUs and to gain extensive information on the internal operation of the controllers. Emulation of on-chip ROM based programs is possible, too.

Each production chip has built-in logic for the support of the Enhanced Hooks Emulation Concept. Therefore, no costly bond-out chips are necessary for emulation. This also ensure that emulation and production chips are identical.

The Enhanced Hooks Technology™<sup>1)</sup>, which requires embedded logic in the C500 allows the C500 together with an EH-IC to function similar to a bond-out chip. This simplifies the design and reduces costs of an ICE-system. ICE-systems using an EH-IC and a compatible C500 are able to emulate all operating modes of the different versions of the C500 microcontrollers. This includes emulation of ROM, ROM with code rollover and ROMless modes of operation. It is also able to operate in single step mode and to read the SFRs after a break.



**Figure 12**  
**Basic C500 MCU Enhanced Hooks Concept Configuration**

Port 0, port 2 and some of the control lines of the C500 based MCU are used by Enhanced Hooks Emulation Concept to control the operation of the device during emulation and to transfer informations about the program execution and data transfer between the external emulation hardware (ICE-system) and the C500 MCU.

1 "Enhanced Hooks Technology" is a trademark and patent of Metalink Corporation licensed to Infineon Technologies.

### Special Function Registers

The registers reside in the special function register area, with the exception of the Program Counter and the four General Purpose Register banks. The special function register area consists of two portions: the *standard* special function register area and the *mapped* special function register area. Four special function registers of the C513AO (PCON1, VR0, VR1 & VR2) are located in the mapped special function register area. For accessing the mapped special function register area, bit RMAP in special function register SYSCON must be set. All other special function registers of the C513AO are located in the standard special function register area.

#### Special Function Register SYSCON (Address B1<sub>H</sub>)

Reset Value: XX10XXX0<sub>B</sub>

Bit No.	MSB							LSB	SYSCON
	7	6	5	4	3	2	1	0	
B1 <sub>H</sub>	-	-	EALE	RMAP	-	-	-	XMAP	

The functions of the shaded bits are not described in this section.

Bit	Function
RMAP	<p><b>Special function Register MAP bit</b></p> <p>RMAP = 0: The access to the non-mapped (standard) special function register area is enabled.</p> <p>RMAP = 1: The access to the mapped special function register area is enabled.</p>
-	Reserved bits for future use. Read by CPU returns undefined values.

If bit RMAP is set, mapped special function registers can be accessed. This bit is not cleared by hardware automatically.

The forty Special Function Registers (SFRs) in the standard and mapped SFR area include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. The SFRs of the C513AO are listed in **Table 2** and **Table 3**. In **Table 2**, they are organized in groups which refer to the functional blocks of the C513AO. **Table 3** illustrates the contents of the SFRs in numeric order of their addresses.

**Table 2**  
**Special Function Registers - Functional Blocks**

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	<b>E0<sub>H</sub></b> <sup>1)</sup>	00 <sub>H</sub>
	B	B-Register	<b>F0<sub>H</sub></b> <sup>1)</sup>	00 <sub>H</sub>
	DPH	Data Pointer, High Byte	83 <sub>H</sub>	00 <sub>H</sub>
	DPL	Data Pointer, Low Byte	82 <sub>H</sub>	00 <sub>H</sub>
	PSW	Program Status Word Register	<b>D0<sub>H</sub></b> <sup>1)</sup>	00 <sub>H</sub>
	SP	Stack Pointer	81 <sub>H</sub>	07 <sub>H</sub>
	SYSCON <sup>2)</sup>	System Control Register	B1 <sub>H</sub>	XX10XXX0 <sub>B</sub> <sup>3)</sup>
	VR0 <sup>4) 5)</sup>	Version Register 0	FC <sub>H</sub>	C5 <sub>H</sub>
VR1 <sup>4) 5)</sup>	Version Register 1 <sup>6)</sup>	FD <sub>H</sub>	–	
VR2 <sup>4) 5)</sup>	Version Register 2 <sup>7)</sup>	FE <sub>H</sub>	–	
Interrupt System	IE	Interrupt Enable Register	<b>A8<sub>H</sub></b> <sup>1)</sup>	00 <sub>H</sub>
	IP	Interrupt Priority Register	<b>B8<sub>H</sub></b> <sup>1)</sup>	X0000000 <sub>B</sub> <sup>3)</sup>
Ports	P0	Port 0	<b>80<sub>H</sub></b> <sup>1)</sup>	FF <sub>H</sub>
	P1	Port 1	<b>90<sub>H</sub></b> <sup>1)</sup>	FF <sub>H</sub>
	P2	Port 2	<b>A0<sub>H</sub></b> <sup>1)</sup>	FF <sub>H</sub>
	P3	Port 3	<b>B0<sub>H</sub></b> <sup>1)</sup>	FF <sub>H</sub>
Serial Channel (USART)	PCON <sup>2)</sup>	Power Control Register	87 <sub>H</sub>	000X0000 <sub>B</sub>
	SBUF	Serial Channel Buffer Register	99 <sub>H</sub>	XX <sub>H</sub> <sup>3)</sup>
	SCON	Serial Channel Control Register	<b>98<sub>H</sub></b> <sup>1)</sup>	00 <sub>H</sub>
SSC Interface	SSCCON	SSC Control Register	<b>E8<sub>H</sub></b> <sup>1)</sup>	07 <sub>H</sub>
	STB	SSC Transmit Register	E9 <sub>H</sub>	XX <sub>H</sub> <sup>3)</sup>
	SRB	SSC Receive Register	EA <sub>H</sub>	XX <sub>H</sub> <sup>3)</sup>
	SCF	SSC Flag Register	<b>F8<sub>H</sub></b> <sup>1)</sup>	XXXXXX00 <sub>B</sub> <sup>3)</sup>
	SCIEN	SSC Interrupt Enable Register	F9 <sub>H</sub>	XXXXXX00 <sub>B</sub> <sup>3)</sup>
	SSCMOD <sup>8)</sup>	SSC Mode Test Register	EB <sub>H</sub>	00 <sub>H</sub>
Timer 0/ Timer 1	TCON	Timer 0/1 Control Register	<b>88<sub>H</sub></b> <sup>1)</sup>	00 <sub>H</sub>
	TH0	Timer 0, High Byte	8C <sub>H</sub>	00 <sub>H</sub>
	TH1	Timer 1, High Byte	8D <sub>H</sub>	00 <sub>H</sub>
	TL0	Timer 0, Low Byte	8A <sub>H</sub>	00 <sub>H</sub>
	TL1	Timer 1, Low Byte	8B <sub>H</sub>	00 <sub>H</sub>
	TMOD	Timer Mode Register	89 <sub>H</sub>	00 <sub>H</sub>

1) Bit-addressable special function registers

2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

3) "X" means that the value is undefined and the location is reserved

4) This SFR is a mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

5) This SFR is read-only.

6) C513AO-L/2R: 13<sub>H</sub>

C513AO-2E: 83<sub>H</sub>

7) This SFR varies with the step of the microcontroller: for example, 01<sub>H</sub> for the first step

8) This register is only used for test purposes and must not be written during normal operation. Unpredictable results may occur upon a write operation.

**Table 2**  
**Special Function Registers - Functional Blocks (cont'd)**

Block	Symbol	Name	Address	Contents after Reset
Timer 2	T2CON	Timer 2 Control Register	<b>C8<sub>H</sub></b> <sup>1)</sup>	00 <sub>H</sub>
	T2MOD	Timer 2 Mode Register	C9 <sub>H</sub>	XXXXXXXX0 <sub>B</sub> <sup>3)</sup>
	RC2H	Timer 2 Reload/Capture Register, High Byte	CB <sub>H</sub>	00 <sub>H</sub>
	RC2L	Timer 2 Reload/Capture Register, Low Byte	CA <sub>H</sub>	00 <sub>H</sub>
	TH2	Timer 2 High Byte	CD <sub>H</sub>	00 <sub>H</sub>
	TL2	Timer 2 Low Byte	CC <sub>H</sub>	00 <sub>H</sub>
	Watchdog	WDCON	Watchdog Timer Control Register	<b>C0<sub>H</sub></b> <sup>1)</sup>
WDTREL		Watchdog Timer Reload Register	86 <sub>H</sub>	00 <sub>H</sub>
Power Save Mode	PCON <sup>2)</sup>	Power Control Register	87 <sub>H</sub>	000X0000 <sub>B</sub> <sup>3)</sup>
	PCON1 <sup>4)</sup>	Power Control Register 1	88 <sub>H</sub>	0XXXXXXXX <sub>B</sub> <sup>3)</sup>

1) Bit-addressable special function registers

2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

3) "X" means that the value is undefined and the location is reserved

4) This SFR is a mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

5) This SFR is read-only.

6) C513AO-L/2R: 13<sub>H</sub>

C513AO-2E: 83<sub>H</sub>

7) This SFR varies with the step of the microcontroller: for example, 01<sub>H</sub> for the first step

8) This register is only used for test purposes and must not be written during normal operation. Unpredictable results may occur upon a write operation.

**Table 3**  
**Contents of the SFRs, SFRs in Numeric Order of their Addresses**

Addr.	Register	Content after Reset <sup>1)</sup>	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80 <sub>H</sub> <sup>2)</sup>	P0	FF <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
81 <sub>H</sub>	SP	07 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
82 <sub>H</sub>	DPL	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
83 <sub>H</sub>	DPH	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
86 <sub>H</sub>	WDTREL	00 <sub>H</sub>	WDT PSEL	.6	.5	.4	.3	.2	.1	.0
87 <sub>H</sub>	PCON	0XX0-0000 <sub>B</sub>	SMOD	–	–	SD	GF1	GF0	PDE	IDLE
88 <sub>H</sub> <sup>2) 3)</sup>	TCON	00 <sub>H</sub>	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
88 <sub>H</sub> <sup>3)</sup>	PCON1	0XX0-XXXX <sub>B</sub>	EWPD	–	–	–	–	–	–	–
89 <sub>H</sub>	TMOD	00 <sub>H</sub>	GATE	C/T	M1	M0	GATE	C/T	M1	M0
8A <sub>H</sub>	TL0	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
8B <sub>H</sub>	TL1	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
8C <sub>H</sub>	TH0	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
8D <sub>H</sub>	TH1	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
90 <sub>H</sub> <sup>2)</sup>	P1	FF <sub>H</sub>	–	–	.SLS	STO	SRI	SCLK	T2EX	T2
98 <sub>H</sub> <sup>2)</sup>	SCON	00 <sub>H</sub>	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99 <sub>H</sub>	SBUF	XX <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
A0 <sub>H</sub> <sup>2)</sup>	P2	FF <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
A8 <sub>H</sub> <sup>2)</sup>	IE	00 <sub>H</sub>	EA	ESSC	ET2	ES	ET1	EX1	ET0	EX0
B0 <sub>H</sub> <sup>2)</sup>	P3	FF <sub>H</sub>	R $\bar{D}$	WR	T1	T0	INT1	INT0	TxD	RxD
B1 <sub>H</sub>	SYSCON	XX10-XXX0 <sub>B</sub>	–	–	EALE	RMAP	–	–	–	XMAP
B8 <sub>H</sub> <sup>2)</sup>	IP	X000-0000 <sub>B</sub>	–	PSSC	PT2	PS	PT1	PX1	PT0	PX0
C0 <sub>H</sub> <sup>2)</sup>	WDCON	XXXX-0000 <sub>B</sub>	–	–	–	–	OWDS	WDS	WDT	SWDT

- 1) "X" means that the value is undefined and the location is reserved.
- 2) Bit-addressable special function registers.
- 3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.
- 4) These are read-only registers.
- 5) The content of this SFR varies with the actual step of the C513AO: for example, 01<sub>H</sub> for the first step).
- 6) This register is only used for test purposes and must not be written during normal operation. Unpredictable results may occur upon a write operation.

**Table 3**  
**Contents of the SFRs, SFRs in Numeric Order of their Addresses (cont'd)**

Addr.	Register	Content after Reset <sup>1)</sup>	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C8 <sub>H</sub> <sup>2)</sup>	T2CON	00 <sub>H</sub>	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/ $\overline{\text{T2}}$	CP/RL2
C9 <sub>H</sub>	T2MOD	XXXX-XXX0 <sub>B</sub>	–	–	–	–	–	–	–	DCEN
CA <sub>H</sub>	RC2L	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
CB <sub>H</sub>	RC2H	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
CC <sub>H</sub>	TL2	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
CD <sub>H</sub>	TH2	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
D0 <sub>H</sub> <sup>2)</sup>	PSW	00 <sub>H</sub>	CY	AC	F0	RS1	RS0	OV	F1	P
E0 <sub>H</sub> <sup>2)</sup>	ACC	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
E8 <sub>H</sub> <sup>2)</sup>	SSCCON	07 <sub>H</sub>	SCEN	TEN	MSTR	CPOL	CPHA	BRS2	BRS1	BRS0
E9 <sub>H</sub>	STB	XX <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
EA <sub>H</sub>	SRB	XX <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
EB <sub>H</sub>	SSCMOD	00 <sub>H</sub> <sup>6)</sup>	LOOPB	TRIO	0	0	0	0	0	LSBSM
F0 <sub>H</sub> <sup>2)</sup>	B	00 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
F8 <sub>H</sub> <sup>2)</sup>	SCF	XXXX-XX00 <sub>B</sub>	–	–	–	–	–	–	WCOL	TC
F9 <sub>H</sub>	SCIEN	XXXX-XX00 <sub>B</sub>	–	–	–	–	–	–	WCEN	TCEN
FC <sub>H</sub> <sup>3) 4)</sup>	VR0	C5 <sub>H</sub>	.7	.6	.5	.4	.3	.2	.1	.0
FD <sub>H</sub> <sup>3) 4)</sup>	VR1	– <sup>7)</sup>	.7	.6	.5	.4	.3	.2	.1	.0
FE <sub>H</sub> <sup>3) 4)</sup>	VR2	– <sup>5)</sup>	.7	.6	.5	.4	.3	.2	.1	.0

1) "X" means that the value is undefined and the location is reserved

2) Bit-addressable special function registers

3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

4) These SFRs are read-only registers.

5) The content of this SFR varies with the actual step of the C513AO: for example, 01<sub>H</sub> for the first step)

6) This register is only used for test purposes and must not be written during normal operation. Unpredictable results may occur upon a write operation.

7) C513AO-L/2R: 13<sub>H</sub>  
 C513AO-2E: 83<sub>H</sub>



### Parallel I/O Port

The C513AO has four 8-bit I/O ports. Port 0 is an open-drain bidirectional I/O port, while Ports 1, 2, and 3 are quasi-bidirectional I/O ports with internal pull-up resistors. Thus, when configured as inputs, Ports 1 to 3 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

The output drivers of Port 0 and Port 2 and the input buffers of Port 0 are also used for accessing external memory. In this application, Port 0 outputs the low byte of the external memory address, time multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise, the Port 2 pins continue to emit the P2 SFR contents. In this case, Port 0 is not an open-drain port, but uses a strong internal pull-up Field Effect Transistors (FETs).

Port 1 pins used for Synchronous Serial Channel (SSC) outputs are true push-pull outputs. When used as SSC inputs, they float (no pull-up).

**Timer/Counter 0 and 1**

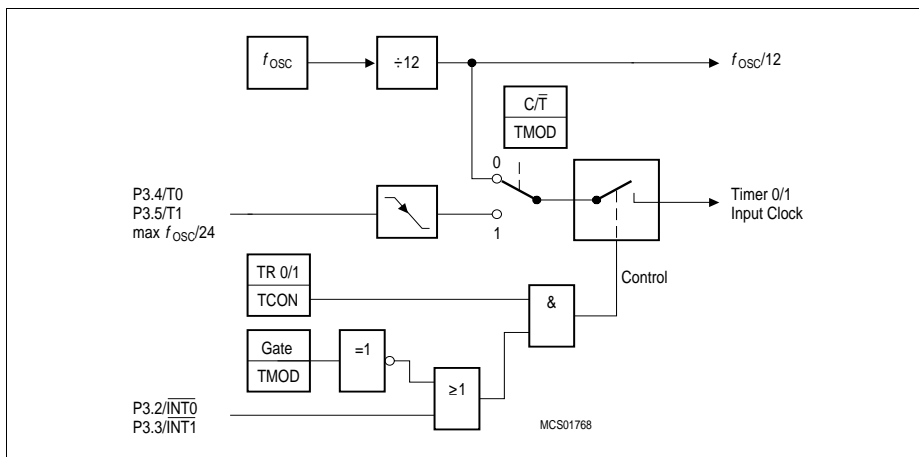
Timer/Counter 0 and 1 can be used in four operating modes as listed in **Table 4**:

**Table 4**  
**Timer/Counter 0 and 1 Operating Modes**

Mode	Description	TMOD		Input Clock	
		M1	M0	Internal	External (max.)
0	8-bit timer/counter with a divide-by-32 prescaler	0	0	$f_{osc}/(12 \times 32)$	$f_{osc}/(24 \times 32)$
1	16-bit timer/counter	1	1	$f_{osc}/12$	$f_{osc}/24$
2	8-bit timer/counter with 8-bit autoreload	1	0		
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	1	1		

In the “timer” function ( $C/\bar{T} = '0'$ ) the register is incremented every machine cycle. Since a machine cycle consists of twelve oscillator periods, the count rate is 1/12th of the oscillator frequency.

In “counter” function, the register is incremented in response to a 1-to-0 transition (falling edge) at its corresponding external input pin, T0 or T1 (alternate functions of P3.4 and P3.5, respectively). Since it takes two machine cycles to detect a falling edge; therefore, the maximum count rate is 1/24th of the oscillator frequency. External inputs  $\overline{INT0}$  and  $\overline{INT1}$  (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 13** illustrates the input clock logic.



**Figure 13**  
**Timer/Counter 0 and 1 Input Clock Logic**

**Timer/Counter 2 with Compare/Capture/Reload**

Timer 2 is a 16-bit timer/counter with an up/down count feature. It has three operating modes:

- 16-bit auto-reload mode (up or down counting)
- 16-bit capture mode
- Baudrate generator

**Table 5**  
**Timer / Counter 2 Operating Modes**

Mode	T2CON			T2MOD	T2CON	P1.1/ T2EX	Remarks	Input Clock	
	RCLK or TCLK	CP/ RL2	TR2	DCEN	EXEN2	Internal		External (P1.0/ T2)	
16-bit Auto- reload	0	0	1	0	0	X	reload upon overflow	$f_{osc}/12$	max $f_{osc}/24$
	0	0	1	0	1	↓	reload trigger (falling edge)		
	0	0	1	1	X	0	down counting		
	0	0	1	1	X	1	up counting		
16-bit Capture	0	1	1	X	0	X	16-bit Timer/ Counter (only up-counting)	$f_{osc}/12$	max $f_{osc}/24$
	0	1	1	X	1	↓	capture TH2, TL2 → RC2H, RC2L		
Baudrate Generator	1	X	1	X	0	X	no overflow interrupt	$f_{osc}/12$	max $f_{osc}/24$
	1	X	1	X	1	↓	request (TF2) extra external interrupt ("Timer 2")		
off	X	X	0	X	X	X	Timer 2 stops	–	–

**Note:** ↓ denotes a falling edge

**Serial Interface (USART)**

The serial port is a full duplex port capable of simultaneous transmit and receive functions. It is also receive-buffered; it can commence reception of a second byte before a previously-received byte has been read from the receive register. The serial port can operate in 4 modes (one synchronous and three asynchronous) as illustrated in **Table 6**.

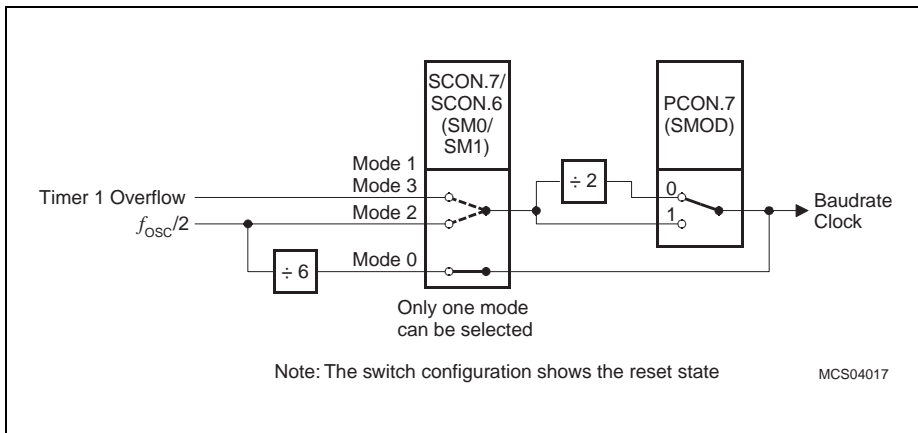
**Table 6**  
**USART Operating Modes**

Mode	SCON		Description
	SM0	SM1	
0	0	0	Shift register mode Serial data enters and exits through RxD. TxD outputs the shift clock. 8-bit data are transmitted/received (LSB first) at a fixed baudrate of $1/12$ th of the oscillator frequency.
1	0	1	8-bit USART, variable baudrate 10 bits are transmitted (through TxD) or received (at RxD).
2	1	0	9-bit USART, fixed baudrate 11 bits are transmitted (through TxD) or received (at RxD).
3	1	1	9-bit USART, variable baudrate Similar to mode 2, except for the variable baudrate.

For clarification, some terms regarding the difference between “baudrate clock” and “baudrate” should be mentioned.

The serial interface requires a clock rate which is 16 times the baudrate for internal synchronization. Therefore, the baudrate generators must provide a “baudrate clock” to the serial interface which divides it by 16, thereby resulting in the actual “baudrate”.

The baudrates in Mode 1 and 3 are determined by the timer overflow rate. These baudrates can be determined by Timer 1 or by Timer 2 or both (one for transmit, the other for receive).



**Figure 14**  
**Block Diagram of Baudrate Generation for the Serial Interface**

**Table 7** lists the values/formulas for the baudrate calculation of the serial interface with its dependencies on the control bits SMOD (in SFR PCON), TCLK and RCLK (both in SFR T2CON).

**Table 7**  
**Serial Interface - Baudrate Dependencies**

Serial Interface Operating Modes	Control Bits		Baudrate Calculation
	SMOD	TCLK/RCLK	
Mode 0 (Shift Register)	–	–	$f_{osc}/12$
Mode 1 (8-bit UART) Mode 3 (9-bit UART)	X	0	Determined by timer 1 overflow rate: $(2^{SMOD} \times \text{timer 1 overflow rate})/32$
	–	1	Determined by timer 2 overflow rate: Timer 2 overflow rate/16
Mode 2 (9-bit UART)	0	–	$f_{osc}/64$
	1	–	$f_{osc}/32$

### SSC Interface

The Synchronous Serial Channel (SSC) interface is compatible to the popular SPI serial bus interface. It can be used for simple I/O expansion via shift registers, for connection with a variety of peripheral components (such as A/D converters, EEPROMs etc.), or interconnection of several microcontrollers in a master/slave structure. The SSC unit supports full-duplex or half-duplex operation and can run in Master Mode or Slave Mode.

Figure 15 shows the block diagram of the SSC.

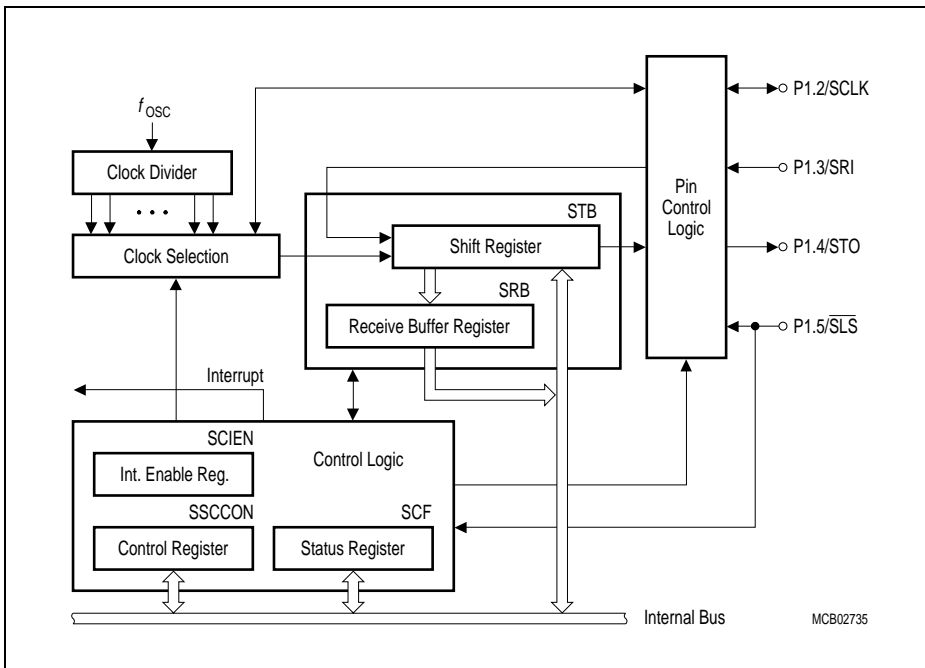


Figure 15  
SSC Block Diagram

### Interrupt System

The C513AO provides seven interrupt sources with two priority levels. Five of the interrupts can be generated by the on-chip peripherals (Timer 0, Timer 1, Timer 2, USART, and SSC) and three of the interrupts may be triggered externally (P1.1/T2EX, P3.2/INT0, P3.3/INT1). A non-maskable eighth interrupt is reserved for external wake-up from power-down mode.

Figure 16 gives a general overview of the interrupt sources and illustrates the request and the control flags. Table 8 lists the vector addresses of each interrupt source.




**Table 8**  
**Interrupt Vector Addresses**

Interrupt Source	Request Flags	Vector Address
External interrupt 0	IE0	0003 <sub>H</sub>
Timer 0 interrupt	TF0	000B <sub>H</sub>
External interrupt 1	IE1	0013 <sub>H</sub>
Timer 1 interrupt	TF1	001B <sub>H</sub>
USART serial port interrupt	RI + TI	0023 <sub>H</sub>
Timer 2 interrupt	TF2 + EXF2	002B <sub>H</sub>
Synchronous Serial Channel interrupt (SSC)	WCOL+TC	0043 <sub>H</sub>
Wake-up from power-down mode	–	007B <sub>H</sub>

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus, within each priority level there is a second priority structure determined by the polling sequence as shown in **Table 9**.

**Table 9**  
**Interrupt Source Structure**

Interrupt Source	Priority
External Interrupt 0	High    Low
Synchronous Serial Channel	
Timer 0 Interrupt	
External Interrupt 1	
Timer 1 Interrupt	
Universal Serial Channel	
Timer 2 Interrupt	

A low-priority interrupt can be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.





## Oscillator Watchdog

The Oscillator Watchdog (OWD) unit is used for three functions:

- **Monitoring the on-chip oscillator's function**

The watchdog supervises the on-chip oscillator's frequency. If the frequency is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is brought into reset. If the failure condition disappears (that is, if the on-chip oscillator has a higher frequency than the RC oscillator), the device executes a final reset phase of typically 1 ms to allow the oscillator to stabilize. Then, the oscillator watchdog reset is released and the device resumes program execution.

- **Fast internal reset after power-on**

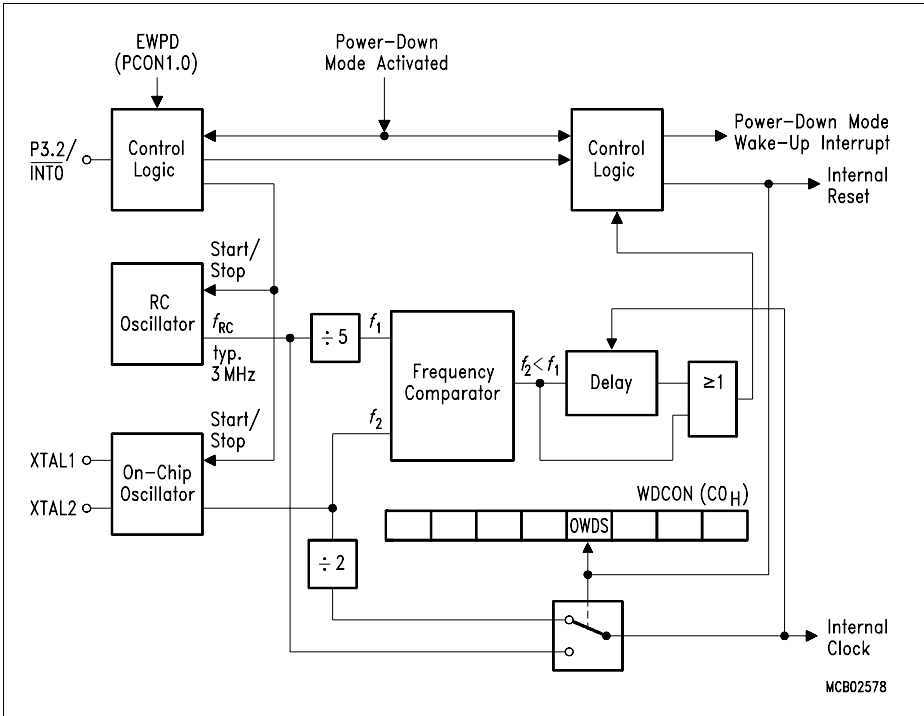
The oscillator watchdog unit provides a clock supply for reset before the on-chip oscillator has started. The oscillator watchdog unit reset works identically to the monitoring function.

- **Control of external wake-up from software power-down mode**

When power-down mode is terminated by a low level at the  $\overline{\text{INT0}}$  pin, the oscillator watchdog unit ensures that the microcontroller resumes operation (execution of the power-down wake-up interrupt) with the nominal clock rate. In power-down mode, the RC oscillator and the on-chip oscillator are stopped. Both oscillators are started again when power-down mode is terminated. When the on-chip oscillator has a frequency higher than the RC oscillator, the microcontroller starts operation after a final delay of typ. 1 ms to allow the on-chip oscillator to stabilize.

**Note:** The Oscillator Watchdog unit is always enabled.

**Figure 18** shows the block diagram of the Oscillator Watchdog unit.



MCB02578

**Figure 18**  
**Block Diagram of the Oscillator Watchdog**

## Power Saving Modes

The C513AO provides three basic power-saving modes: Idle Mode, Slow-down Mode, and Power-down Mode.

- **Idle mode**

The CPU is gated off from the oscillator. All peripherals are still provided with the clock and are able to function. Idle mode is entered by software and can be left by an interrupt or reset.

- **Slow down mode**

The controller keeps up the full operating functionality, but its normal clock frequency is internally divided by 32. This slows down all parts of the controller, the CPU and all peripherals, to 1/32nd of their normal operating frequency and also reduces power consumption.

- **Power down mode**

The operation of the C513AO is completely stopped and the oscillator is turned off. This mode is used to save the contents of the internal RAM with a very low standby current. This power down mode is entered by software and can be left by reset or a short low pulse at pin P3.2/INT0.

In the power down mode of operation,  $V_{DD}$  can be reduced to minimize power consumption. It must be ensured, however, that  $V_{DD}$  is not reduced before the power down mode is invoked, and that  $V_{DD}$  is restored to its normal operating level, before the power down mode is terminated. **Table 10** gives a general overview of the entry and exit procedures of the power saving modes.

**Table 10**  
**Power Saving Modes Overview**

Mode	Entering Example	Leaving by	Remarks
Idle mode	ORL PCON, #01 <sub>H</sub>	Occurrence of an any enabled interrupt	CPU clock is stopped; CPU maintains their data; peripheral units are active (if enabled) and provided with clock
		Hardware reset	
Slow Down Mode	In normal mode: ORL PCON, #10 <sub>H</sub>	ANL PCON, #0EF <sub>H</sub> or Hardware reset	Internal clock rate is reduced to 1/32 of its nominal frequency
	With idle mode: ORL PCON, #11 <sub>H</sub>	Occurrence of any enabled interrupt and the instruction ANL PCON, #0EF <sub>H</sub>	CPU clock is stopped; CPU maintains their data; peripheral units are active (if enabled) and provided with 1/32 of its nominal frequency
		Hardware reset	
Power Down Mode	ORL PCON, #02 <sub>H</sub>	Hardware reset	Oscillator is stopped; contents of on-chip RAM and SFRs are maintained;
		Short low pulse at pin P3.2/INT0	

**Absolute Maximum Ratings**

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	$T_{ST}$	- 65	150	°C	-
Voltage on $V_{DD}$ pins with respect to ground ( $V_{SS}$ )	$V_{DD}$	- 0.5	6.5	V	-
Voltage on any pin with respect to ground ( $V_{SS}$ )	$V_{IN}$	- 0.5	$V_{DD} + 0.5$	V	-
Input current on any pin during overload condition	-	- 10	10	mA	-
Absolute sum of all input currents during overload condition	-	-	100 mA	mA	-
Power dissipation	$P_{DISS}$	-	t.b.d.	W	-

**Note:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During absolute maximum rating overload conditions ( $V_{IN} > V_{DD}$  or  $V_{IN} < V_{SS}$ ) the voltage on  $V_{DD}$  pins with respect to ground ( $V_{SS}$ ) must not exceed the values defined by the absolute maximum ratings.

**Operating Conditions**

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply voltage	$V_{DD}$	4.25	5.5	V	-
Ground voltage	$V_{SS}$	0		V	-
Ambient temperature				°C	-
SAB-C513AO	$T_A$	0	70		
SAF-C513AO	$T_A$	- 40	85		
CPU clock	$f_{CPU}$	3.5	16	MHz	-

### Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C513AO and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

#### CC (Controller Characteristics):

The logic of the C513AO will provide signals with the respective characteristics.

#### SR (System Requirement):

The external system must provide signals with the respective characteristics to the C513AO.

### DC Characteristics

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage Pins except EA, RESET	$V_{IL}$ SR	-0.5	$0.2 V_{DD} - 0.1$	V	-
EA pin	$V_{IL1}$ SR	-0.5	$0.2 V_{DD} - 0.3$	V	-
RESET pin	$V_{IL2}$ SR	-0.5	$0.2 V_{DD} + 0.1$	V	-
Input high voltage Pins except XTAL1, RESET	$V_{IH}$ SR	$0.6 V_{DD}$	$V_{DD} + 0.5$	V	-
XTAL1 pin	$V_{IH1}$ SR	$0.7 V_{DD}$	$V_{DD} + 0.5$	V	-
RESET pin	$V_{IH2}$ SR	$0.6 V_{DD}$	$V_{DD} + 0.5$	V	-
Output low voltage Ports 1, 2, 3 (except P1.2, P1.4)	$V_{OL}$ CC	-	0.45	V	$I_{OL} = 1.6 \text{ mA}^1$
Port 0, ALE, $\overline{\text{PSEN}}$	$V_{OL1}$ CC	-	0.45	V	$I_{OL} = 3.2 \text{ mA}^1$
P1.2, P1.4 pull-up transistor resistance	$R_{DSON}$ CC	-	120	$\Omega$	$V_{OL} = 0.45 \text{ V}$
Output High Voltage Ports 1, 2, 3	$V_{OH}$ CC	2.4	-	V	$I_{OH} = -80 \mu\text{A}$ ,
		$0.9 V_{DD}$	-	V	$I_{OH} = -10 \mu\text{A}$
Port 0 in external bus mode, ALE, $\overline{\text{PSEN}}$	$V_{OH1}$ CC	2.4	-	V	$I_{OH} = -800 \mu\text{A}$ ,
		$0.9 V_{DD}$	-	V	$I_{OH} = -80 \mu\text{A}^2$
P1.2, P1.4 pull-up transistor resistance	$R_{DSON}$ CC	-	120	$\Omega$	$V_{OH} = 0.9 V_{DD}$
Logic 0 input current Ports 1, 2, 3	$I_{IL}$ SR	-10	-70	$\mu\text{A}$	$V_{IN} = 0.45 \text{ V}$
Logical 0-to-1 transition current, Ports 1, 2, 3	$I_{TL}$ SR	-65	-650	$\mu\text{A}$	$V_{IN} = 2 \text{ V}$
Input Leakage Current Port 0, EA P1.2, P1.3, P1.5 as SSC inputs	$I_{LI}$ CC	-	$\pm 1$	$\mu\text{A}$	$0.45 < V_{IN} < V_{DD}$
Input high current to RESET for reset	$I_{IH}$ CC	5	100	$\mu\text{A}$	$0.6 < V_{IN} < V_{DD}$

**DC Characteristics (cont'd)**  
 (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low current to XTAL1	$I_{IL2}$ CC	–	– 20	μA	$V_{IN} = 0.45$ V
Pin capacitance	$C_{IO}$ CC	–	10	pF	$f_C = 1$ MHz, $T_A = 25$ °C
Overload current	$I_{OV}$ SR	–	± 5	mA	<sup>8)</sup> <sup>9)</sup>

Notes see next page.

**Power Supply Current**

Parameter			Symbol	Limit Values		Unit	Test Condition
				typ. <sup>10)</sup>	max.		
Active mode	C513AO-2E	12 MHz	$I_{DD}$	10.3	13.0	mA	4)
		16 MHz	$I_{DD}$	13.1	16.6	mA	
	C513AO-2R	12 MHz	$I_{DD}$	6.9	9.0	mA	4)
		16 MHz	$I_{DD}$	8.5	10.9	mA	
Idle mode	C513AO-2E	12 MHz	$I_{DD}$	5.7	7.2	mA	5)
		16 MHz	$I_{DD}$	6.8	8.7	mA	
	C513AO-2R	12 MHz	$I_{DD}$	4.1	5.5	mA	5)
		16 MHz	$I_{DD}$	4.8	6.0	mA	
Active mode with slow-down enabled	C513AO-2E	12 MHz	$I_{DD}$	4.5	5.7	mA	6)
		16 MHz	$I_{DD}$	5.1	6.5	mA	
	C513AO-2R	12 MHz	$I_{DD}$	3.3	4.1	mA	6)
		16 MHz	$I_{DD}$	3.6	4.5	mA	
Idle mode with slow-down enabled	C513AO-2E	12 MHz	$I_{DD}$	3.7	4.7	mA	7)
		16 MHz	$I_{DD}$	4.0	5.1	mA	
	C513AO-2R	12 MHz	$I_{DD}$	2.6	3.3	mA	7)
		16 MHz	$I_{DD}$	2.8	3.5	mA	
Power-down mode	C513AO-2E		$I_{PD}$	8.8	50	μA	$V_{DD} = 2 \dots 5.5$ V <sup>3)</sup>
	C513AO-2R		$I_{PD}$	1.28	20	μA	$V_{DD} = 2 \dots 5.5$ V <sup>3)</sup>

**Notes:**

- 1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the  $V_{OL}$  of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a Schmitt-trigger, or use an address latch with a Schmitt-trigger strobe input.
- 2) Capacitive loading on ports 0 and 2 may cause the  $V_{OH}$  on ALE and PSEN to momentarily fall below the 0.9  $V_{DD}$  specification when the address lines are stabilizing.
- 3)  $I_{PD}$  (power-down mode) is measured under following conditions:  
EA = Port0 =  $V_{DD}$ ; RESET =  $V_{SS}$ ; XTAL2 = N.C.; XTAL1 =  $V_{SS}$ ; all other pins are disconnected.  $I_{DD}$  would be slightly higher if a crystal oscillator is used (appr. 1 mA).
- 4)  $I_{DD}$  (active mode) is measured with:  
XTAL2 driven with  $t_{CLCH}$ ,  $t_{CHCL}$  = 5 ns,  $V_{IL}$  =  $V_{SS} + 0.5$  V,  $V_{IH}$  =  $V_{DD} - 0.5$  V; XTAL1 = N.C.;  
EA =  $\overline{PE}/SWD$  = Port 0 = Port 6 =  $V_{DD}$ ;  $\overline{HWPD}$  =  $V_{DD}$ ; RESET =  $V_{DD}$ ;  
all other pins are disconnected.  $I_{DD}$  would be slightly higher if a crystal oscillator is used (appr. 1 mA).
- 5)  $I_{DD}$  (idle mode) is measured with all output pins disconnected and with all peripherals disabled;  
XTAL1 driven with  $t_{CLCH}$ ,  $t_{CHCL}$  = 5 ns,  $V_{IL}$  =  $V_{SS} + 0.5$  V,  $V_{IH}$  =  $V_{DD} - 0.5$  V; XTAL2 = N.C.;  
RESET =  $\overline{EA}$  =  $V_{SS}$ ; Port0 =  $V_{DD}$ ; all other pins are disconnected.
- 6)  $I_{DD}$  (active mode with slow-down mode) is measured with all output pins disconnected and with all peripherals disabled; XTAL1 driven with  $t_{CLCH}$ ,  $t_{CHCL}$  = 5 ns,  $V_{IL}$  =  $V_{SS} + 0.5$  V,  $V_{IH}$  =  $V_{DD} - 0.5$  V; XTAL2 = N.C.;  
RESET =  $\overline{EA}$  =  $V_{SS}$ ; Port0 =  $V_{DD}$ ; all other pins are disconnected.
- 7)  $I_{DD}$  (idle mode with slow-down mode) is measured with all output pins disconnected and with all peripherals disabled; XTAL1 driven with  $t_{CLCH}$ ,  $t_{CHCL}$  = 5 ns,  $V_{IL}$  =  $V_{SS} + 0.5$  V,  $V_{IH}$  =  $V_{DD} - 0.5$  V; XTAL2 = N.C.;  
RESET =  $\overline{EA}$  =  $V_{SS}$ ; Port0 =  $V_{DD}$ ; all other pins are disconnected.
- 8) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e.  $V_{OV} > V_{DD} + 0.5$  V or  $V_{OV} < V_{SS} - 0.5$  V). The supply voltage  $V_{DD}$  and  $V_{SS}$  must remain within the specified limits. The absolute sum of input currents on all port pins may not exceed 50 mA.
- 9) Not 100% tested, guaranteed by design characterization.
- 10) The typical  $I_{DD}$  values are periodically measured at  $T_A = +25$  °C and  $V_{DD} = 5$  V but not 100% tested.



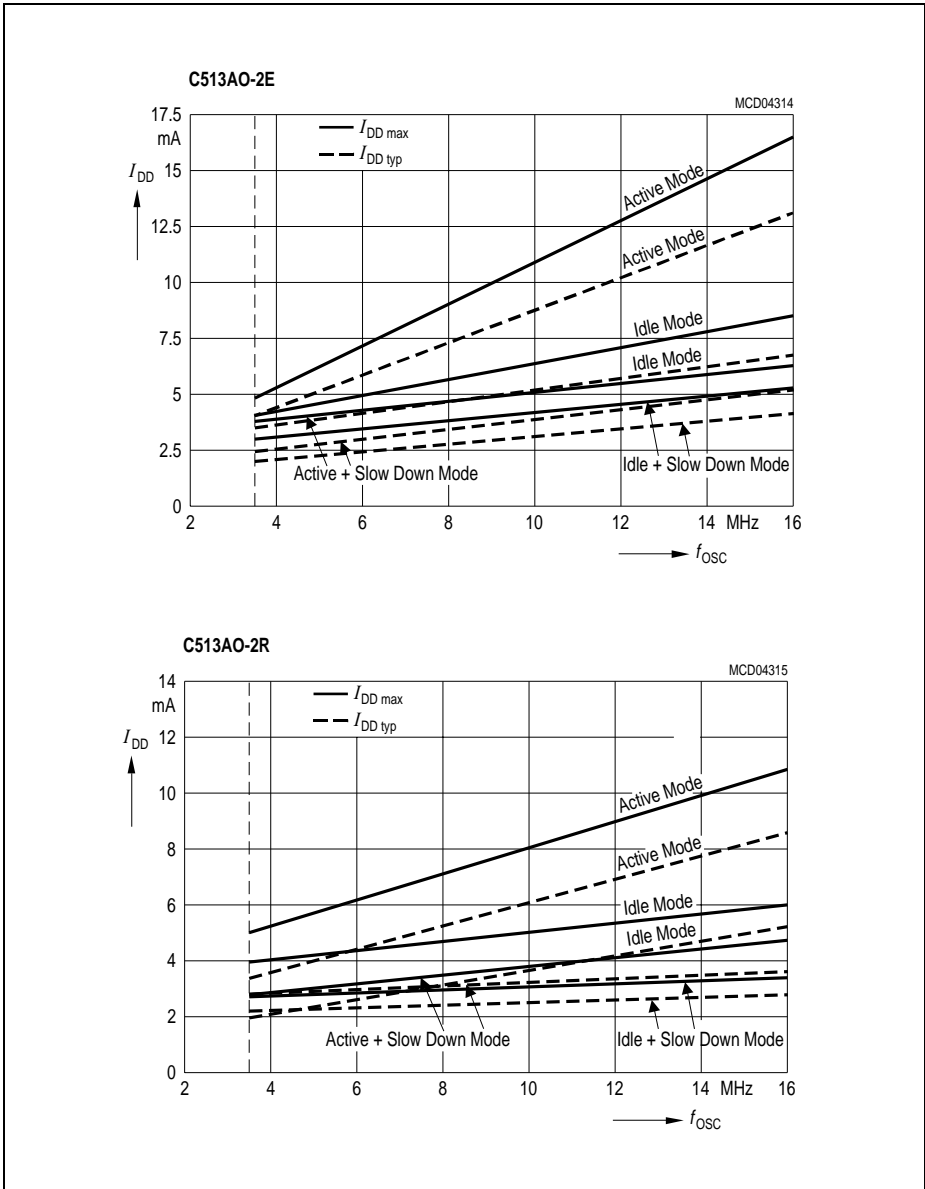


Figure 19  
 $I_{DD}$  Diagram

**Power Supply Current Calculation Formula**

Parameter		Symbol	Formula
Active mode	C513-2E	$I_{DD \text{ typ}}$ $I_{DD \text{ max}}$	$0.70 \times f_{OSC} + 1.8$ $0.91 \times f_{OSC} + 2.0$
	C513-2R	$I_{DD \text{ typ}}$ $I_{DD \text{ max}}$	$0.40 \times f_{OSC} + 2.1$ $0.48 \times f_{OSC} + 3.2$
Idle mode	C513-2E	$I_{DD \text{ typ}}$ $I_{DD \text{ max}}$	$0.29 \times f_{OSC} + 2.2$ $0.36 \times f_{OSC} + 2.9$
	C513-2R	$I_{DD \text{ typ}}$ $I_{DD \text{ max}}$	$0.18 \times f_{OSC} + 1.9$ $0.13 \times f_{OSC} + 3.9$
Active mode with slow-down enabled	C513-2E	$I_{DD \text{ typ}}$ $I_{DD \text{ max}}$	$0.15 \times f_{OSC} + 2.6$ $0.20 \times f_{OSC} + 2.9$
	C513-2R	$I_{DD \text{ typ}}$ $I_{DD \text{ max}}$	$0.08 \times f_{OSC} + 2.4$ $0.10 \times f_{OSC} + 2.9$
Idle mode with slow-down enabled	C513-2E	$I_{DD \text{ typ}}$ $I_{DD \text{ max}}$	$0.09 \times f_{OSC} + 2.5$ $0.12 \times f_{OSC} + 3.2$
	C513-2R	$I_{DD \text{ typ}}$ $I_{DD \text{ max}}$	$0.05 \times f_{OSC} + 2.0$ $0.05 \times f_{OSC} + 2.7$

**Note:**  $f_{OSC}$  is the oscillator frequency in MHz.  $I_{DD}$  values are given in mA.

**AC Characteristics (16 MHz)**

(Operating Conditions apply)

 ( $C_L$  for port 0, ALE and  $\overline{\text{PSEN}}$  outputs = 100 pF;  $C_L$  for all other outputs = 80 pF)

Parameter	Symbol	Limit Values				Unit
		16 MHz Clock		Variable Clock $1/t_{\text{CLCL}} = 3.5 \text{ MHz to } 16 \text{ MHz}$		
		min.	max.	min.	max.	

**Program Memory Characteristics**

ALE pulse width	$t_{\text{LHLL}}$ CC	85	–	$2 t_{\text{CLCL}} - 40$	–	ns
Address setup to ALE	$t_{\text{AVLL}}$ CC	33	–	$t_{\text{CLCL}} - 30$	–	ns
Address hold after ALE	$t_{\text{LLAX}}$ CC	28	–	$t_{\text{CLCL}} - 35$	–	ns
ALE low to valid instruction in	$t_{\text{LLIV}}$ SR	–	150	–	$4 t_{\text{CLCL}} - 100$	ns
ALE to $\overline{\text{PSEN}}$	$t_{\text{LLPL}}$ CC	38	–	$t_{\text{CLCL}} - 25$	–	ns
$\overline{\text{PSEN}}$ pulse width	$t_{\text{PLPH}}$ CC	153	–	$3 t_{\text{CLCL}} - 35$	–	ns
$\overline{\text{PSEN}}$ to valid instruction in	$t_{\text{PLIV}}$ SR	–	88	–	$3 t_{\text{CLCL}} - 100$	ns
Input instruction hold after $\overline{\text{PSEN}}$	$t_{\text{PXIX}}$ SR	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	$t_{\text{PXIZ}}^{*)}$ SR	–	43	–	$t_{\text{CLCL}} - 20$	ns
Address valid after $\overline{\text{PSEN}}$	$t_{\text{PXAV}}^{*)}$ CC	48	–	$t_{\text{CLCL}} - 8$	–	ns
Address to valid instr in	$t_{\text{AVIV}}$ SR	–	198	–	$5 t_{\text{CLCL}} - 115$	ns
Address float to $\overline{\text{PSEN}}$	$t_{\text{AZPL}}$ CC	0	–	0	–	ns

<sup>\*)</sup> Interfacing the C513AO to devices with float times up to 55 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

**AC Characteristics (16 MHz, cont'd)**

(Operating Conditions apply)

 ( $C_L$  for port 0, ALE and PSEN outputs = 100 pF;  $C_L$  for all other outputs = 80 pF)

Parameter	Symbol	Limit Values				Unit
		16 MHz Clock		Variable Clock $1/t_{CLCL} = 3.5 \text{ MHz to } 16 \text{ MHz}$		
		min.	max.	min.	max.	

**External Data Memory Characteristics**

$\overline{RD}$ pulse width	$t_{RLRH}$ CC	275	–	$6 t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	$t_{WLWH}$ CC	275	–	$6 t_{CLCL} - 100$	–	ns
Address hold after ALE	$t_{LLAX2}$ CC	90	–	$2 t_{CLCL} - 35$	–	ns
$\overline{RD}$ to valid data in	$t_{RLDV}$ SR	–	148	–	$5 t_{CLCL} - 165$	ns
Data hold after $\overline{RD}$	$t_{RHDX}$ SR	0	–	0	–	ns
Data float after $\overline{RD}$	$t_{RHDZ}$ SR	–	55	–	$2 t_{CLCL} - 70$	ns
ALE to valid data in	$t_{LLDV}$ SR	–	350	–	$8 t_{CLCL} - 150$	ns
Address to valid data in	$t_{AVDV}$ SR	–	398	–	$9 t_{CLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	$t_{LLWL}$ CC	138	238	$3 t_{CLCL} - 50$	$3 t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	$t_{AVWL}$ CC	120	–	$4 t_{CLCL} - 130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	$t_{WHLH}$ CC	23	103	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns
Data valid to $\overline{WR}$ transition	$t_{QVWX}$ CC	13	–	$t_{CLCL} - 50$	–	ns
Data setup before $\overline{WR}$	$t_{QVWH}$ CC	288	–	$7 t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	$t_{WHQX}$ CC	13	–	$t_{CLCL} - 50$	–	ns
Address float after $\overline{RD}$	$t_{RLAZ}$ CC	–	0	–	0	ns

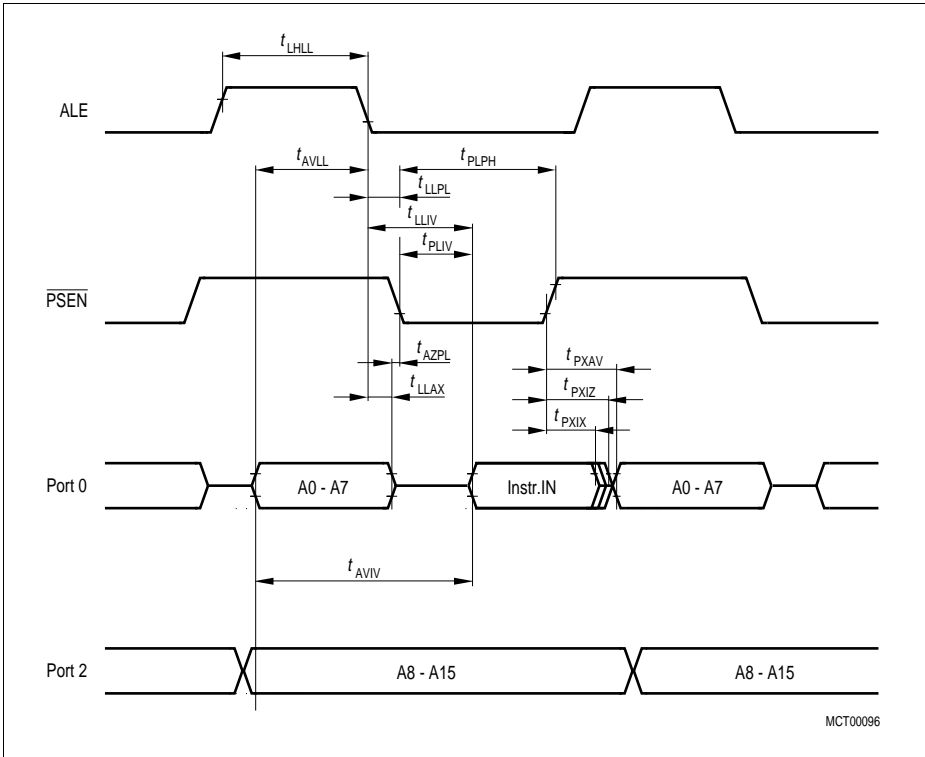
**Synchronous Serial Channel (SSC) Interface Characteristics**

Parameter	Symbol	Limit Values		Unit
		16 MHz Clock		
		min.	max.	
Clock Cycle Time: Master Mode Slave Mode	$t_{SCLK}$ CC	500	–	ns
	$t_{SCLK}$ SR	450	–	ns
Clock High Time	$t_{SCH}$ CC/SR <sup>1)</sup>	200	–	ns
Clock Low Time	$t_{SCL}$ CC/SR <sup>1)</sup>	200	–	ns
Data Output Delay	$t_D$ CC	–	100	ns
Data Output Hold	$t_{HO}$ CC	0	–	ns
Data Input Setup	$t_S$ SR	80	–	ns
Data Input Hold	$t_{HI}$ SR	80	–	ns
TC Bit Set Delay	$t_{DTC}$ CC	–	16 $t_{CLCL}$	ns

1) This parameter is 'CC' in Master Mode, and 'SR' in Slave Mode.

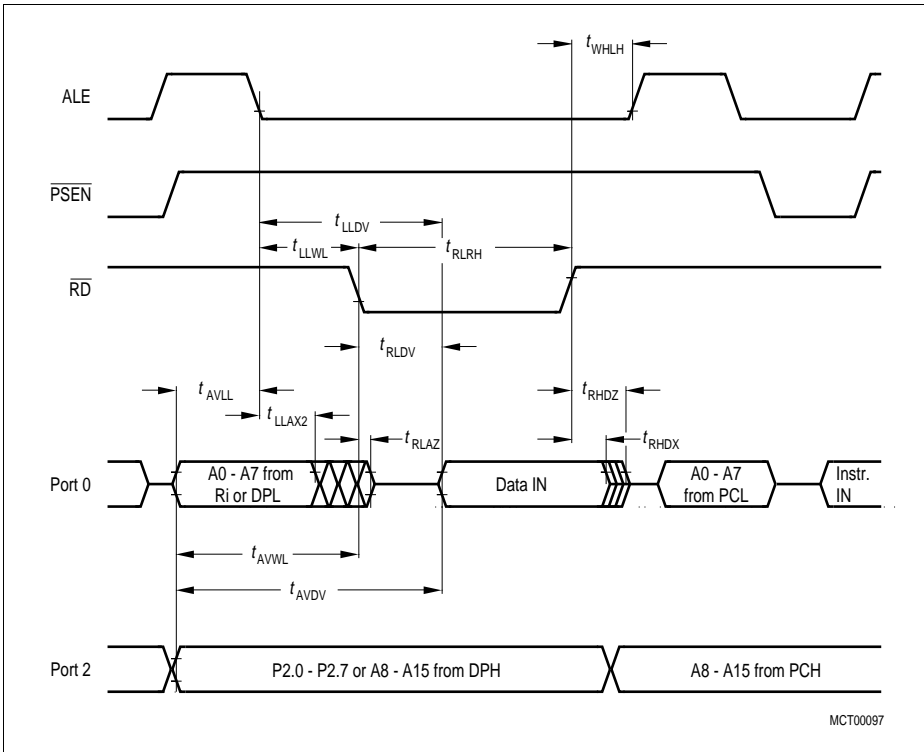
**External Clock Drive Characteristics**

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 16 MHz		
		min.	max.	
Oscillator period	$t_{CLCL}$ SR	62.5	285	ns
High time	$t_{CHCX}$ SR	15	$t_{CLCL} - t_{CLCX}$	ns
Low time	$t_{CLCX}$ SR	15	$t_{CLCL} - t_{CHCX}$	ns
Rise time	$t_{CLCH}$ SR	–	15	ns
Fall time	$t_{CHCL}$ SR	–	15	ns

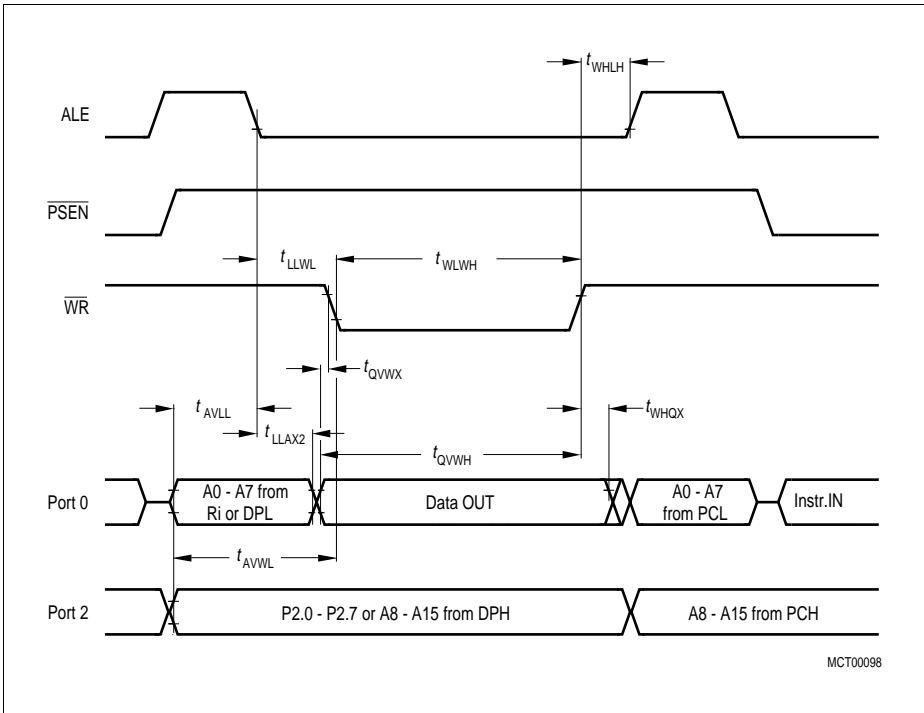


MCT00096

**Figure 20**  
**Program Memory Read Cycle**

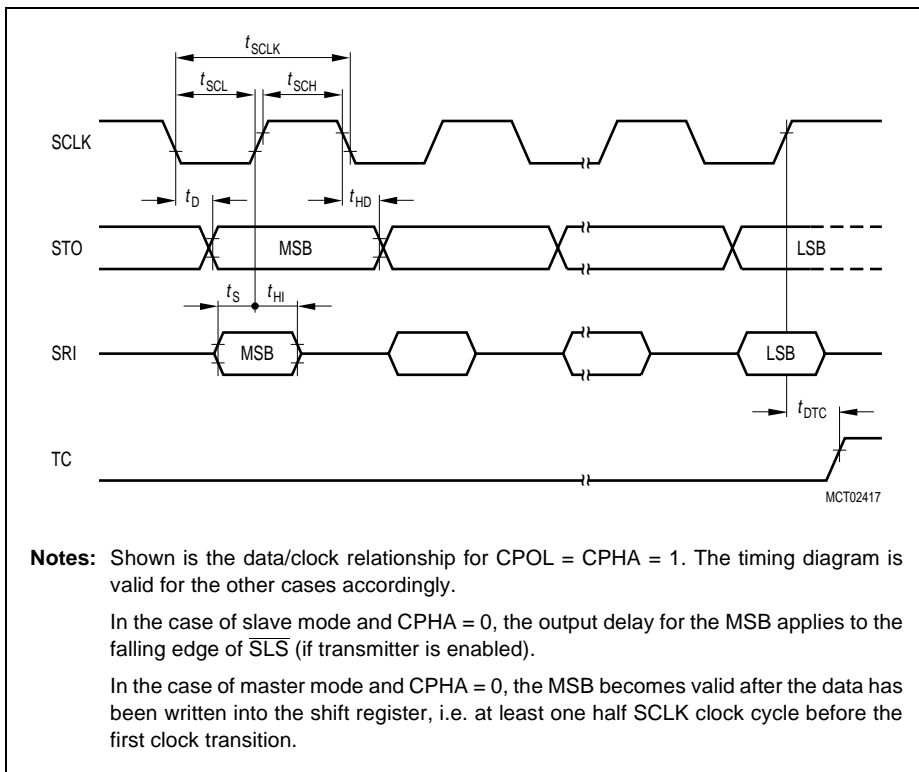


**Figure 21**  
**Data Memory Read Cycle**



**Figure 22**  
Data Memory Write Cycle



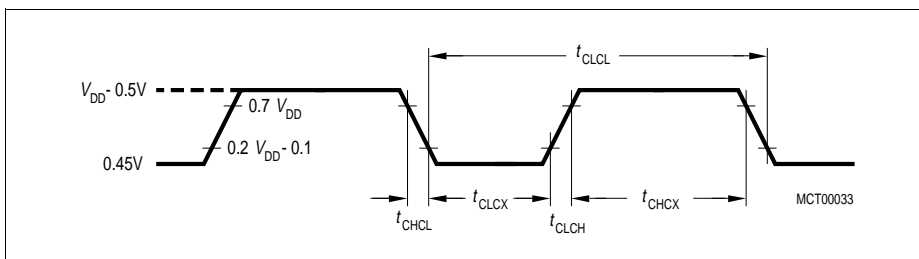


**Notes:** Shown is the data/clock relationship for CPOL = CPHA = 1. The timing diagram is valid for the other cases accordingly.

In the case of slave mode and CPHA = 0, the output delay for the MSB applies to the falling edge of  $\overline{SLS}$  (if transmitter is enabled).

In the case of master mode and CPHA = 0, the MSB becomes valid after the data has been written into the shift register, i.e. at least one half SCLK clock cycle before the first clock transition.

**Figure 23**  
SSC Timing

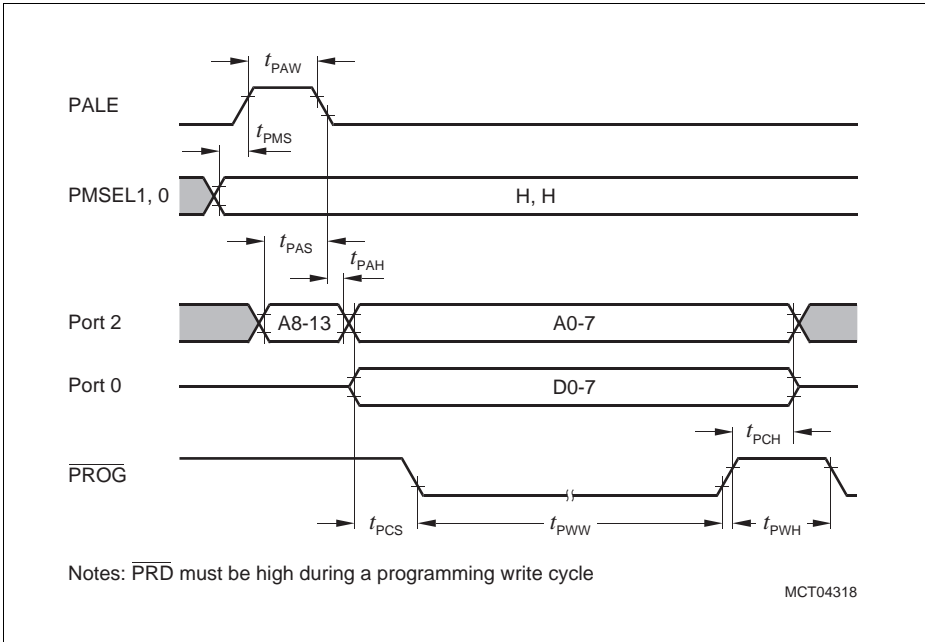


**Figure 24**  
External Clock Drive on XTAL1

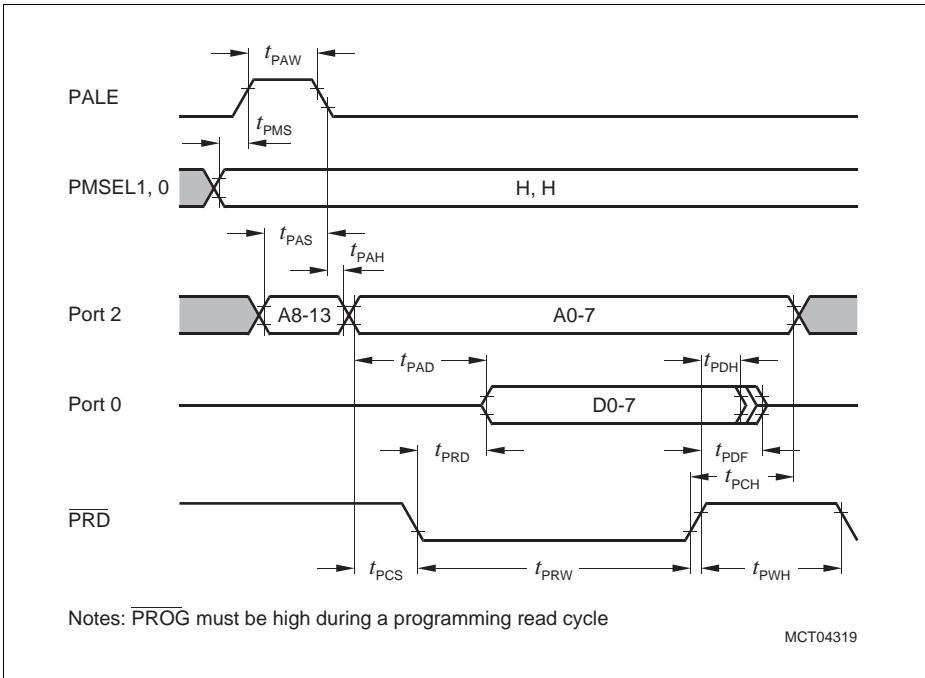
**OTP Memory Characteristics (C513AO-2E only)**
**Programming Mode Timing Characteristics**

(Operating Conditions apply)

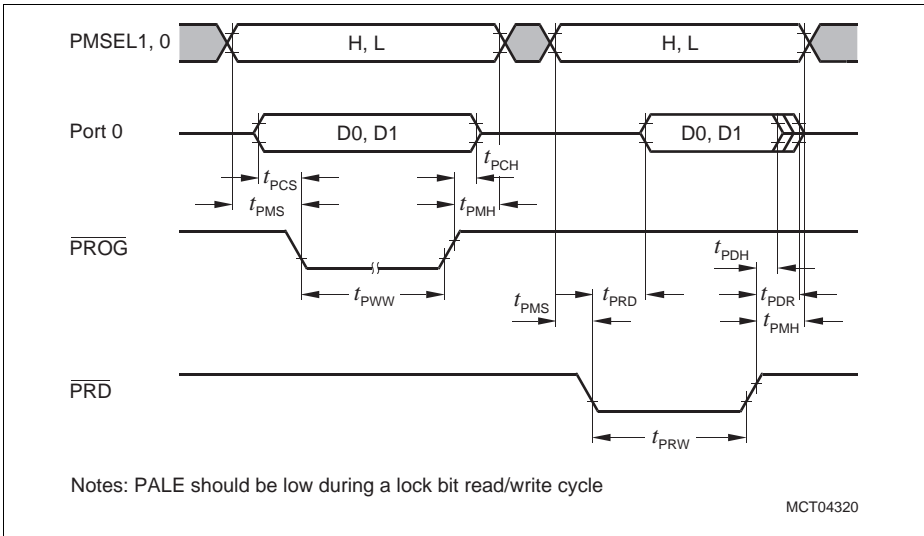
Parameter	Symbol	Limit Values		Unit
		min.	max.	
PALE Pulse Width	$t_{PAW}$	35	–	ns
PMSEL Set-up to PALE Rising Edge	$t_{PMS}$	10	–	–
Address Set-up to PALE, $\overline{PROG}$ , or $\overline{PRD}$ Falling Edge	$t_{PAS}$	10	–	ns
Address Hold after PALE, $\overline{PROG}$ , or $\overline{PRD}$ Falling Edge	$t_{PAH}$	10	–	ns
Address, Data Set-up to $\overline{PROG}$ or $\overline{PRD}$	$t_{PCS}$	100	–	ns
Address, Data Hold after $\overline{PROG}$ or $\overline{PRD}$	$t_{PCH}$	0	–	ns
PMSEL Set-up to $\overline{PROG}$ or $\overline{PRD}$	$t_{PMS}$	10	–	ns
PMSEL Hold after $\overline{PROG}$ or $\overline{PRD}$	$t_{PMH}$	10	–	ns
$\overline{PROG}$ Pulse Width	$t_{PWW}$	100	–	$\mu$ s
$\overline{PRD}$ Pulse Width	$t_{PRW}$	100	–	ns
Address to Valid Data out	$t_{PAD}$	–	75	ns
$\overline{PRD}$ to Valid Data out	$t_{PRD}$	–	20	ns
Data Hold after $\overline{PRD}$	$t_{PDH}$	0	–	ns
Data float after $\overline{PRD}$	$t_{PDF}$	–	20	ns
$\overline{PROG}$ High between two Consecutive $\overline{PROG}$ Low Pulses	$t_{PWH1}$	1	–	$\mu$ s
$\overline{PRD}$ High between two Consecutive $\overline{PRD}$ Low Pulses	$t_{PWH2}$	100	–	ns
XTAL Clock Period	$t_{CLKP}$	62.5	286	ns



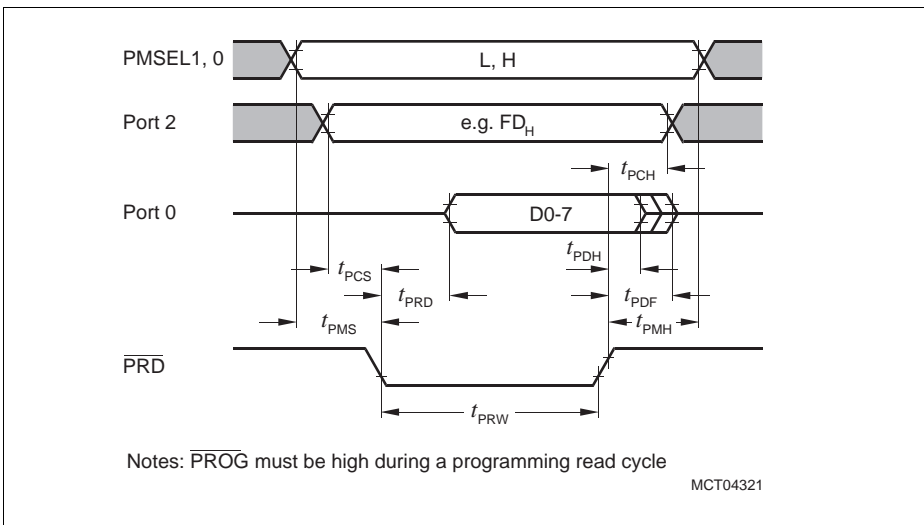
**Figure 25**  
**Programming Code Byte - Write Cycle Timing**



**Figure 26**  
**Verify Code Byte - Read Cycle Timing**



**Figure 27**  
**Lock Bit Access Timing**

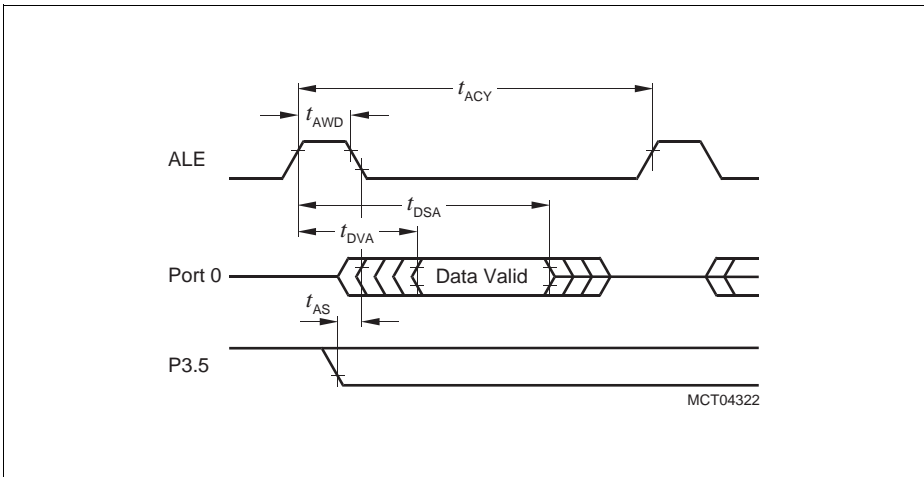


**Figure 28**  
**Version Registers - Read Timing**

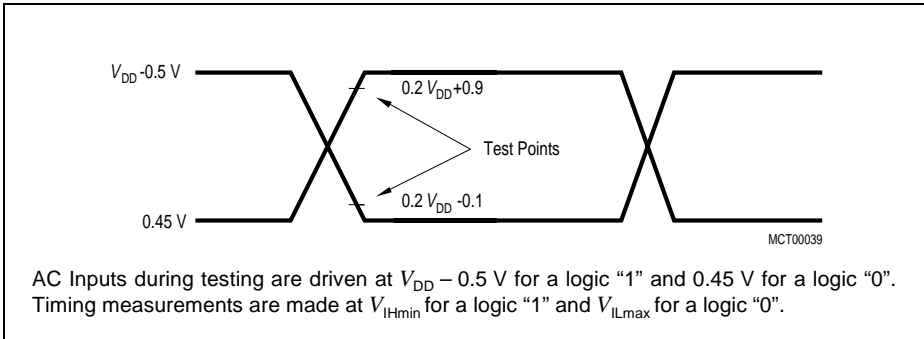
**OTP Verification Mode Characteristics**

**Note:** ALE pin described below is **not** the OTP Programming Mode pin PALE

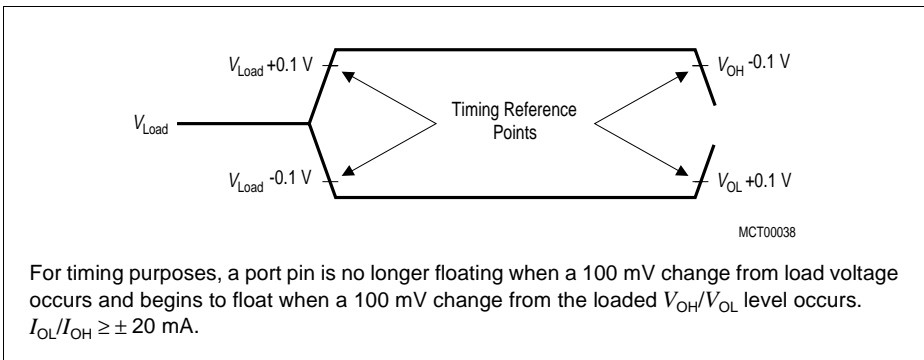
Parameter	Symbol	Limit Values			Unit
		min.	typ	max.	
ALE Pulse Width	$t_{AWD}$	–	$2 t_{CLCL}$	–	ns
ALE Period	$t_{ACY}$	–	$12 t_{CLCL}$	–	ns
Data Valid after ALE	$t_{DVA}$	–	–	$4 t_{CLCL}$	ns
Data Stable after ALE	$t_{DSA}$	$8 t_{CLCL}$	–	–	ns
P3.5 Set-up to ALE Low	$t_{AS}$	–	$t_{CLCL}$	–	ns
Oscillator Frequency	$1/t_{CLCL}$	4	–	6	MHz



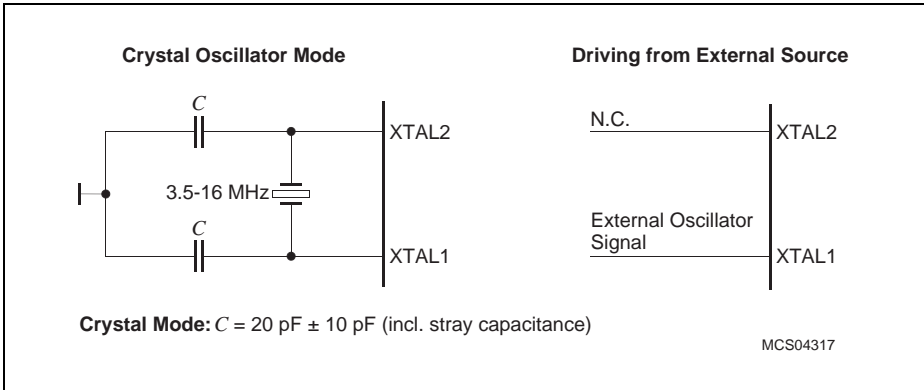
**Figure 29**  
**OTP Verification Mode**



**Figure 30**  
**AC Testing: Input, Output Waveforms**



**Figure 31**  
**AC Testing: Float Waveforms**

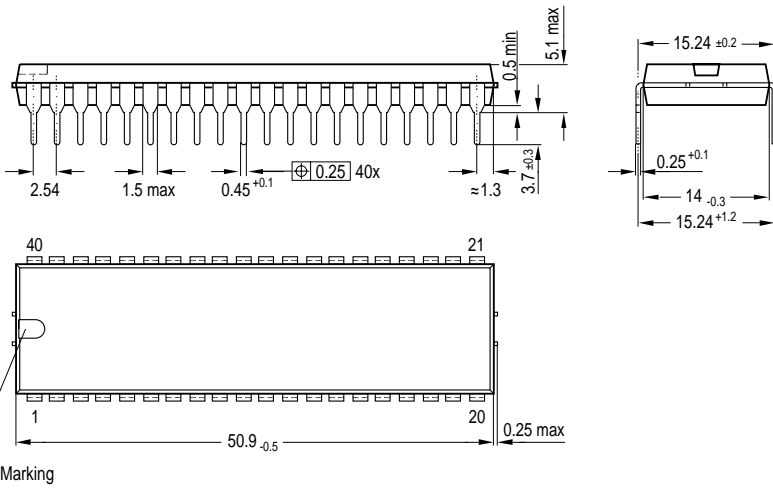


**Figure 32**  
**Recommended Oscillator Circuits for Crystal Oscillator**



Package Outlines

**Plastic Package, P-DIP-40-2**  
(Plastic Dual In-Line Package)



GPD05055

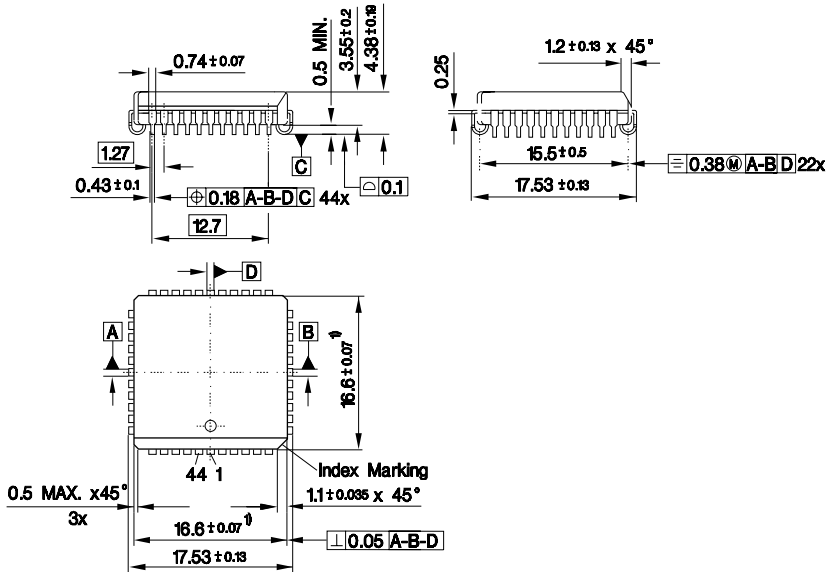
**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

**SMD = Surface Mounted Device**

Dimensions in mm

**Plastic Package, P-LCC-44-1**  
(Plastic Lead Chip Carrier)



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPL05102

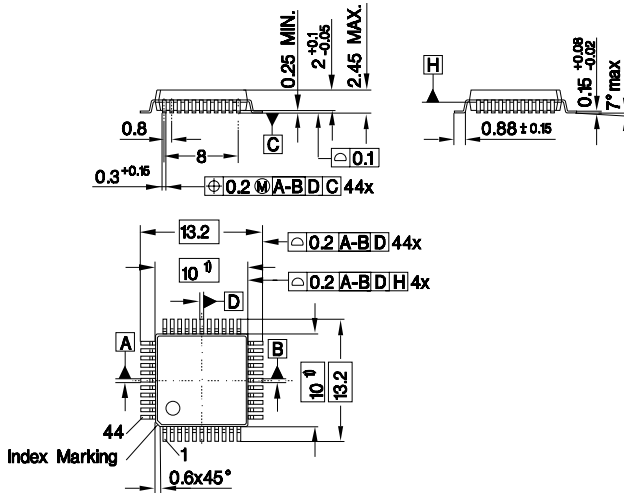
**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

**SMD = Surface Mounted Device**

Dimensions in mm

**Plastic Package, P-MQFP-44-2**  
(Plastic Metric Quad Flat Pack)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPM05622

**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

**SMD = Surface Mounted Device**

Dimensions in mm