National Semiconductor

PRELIMINARY

DP84300 Programmable Refresh Timer

General Description

The DP84300 programmable refresh timer is a logic device which produces the desired refresh clock required by all dynamic memory systems.

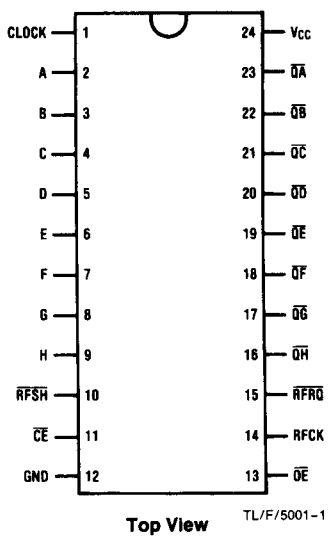
Additional circuitry has been included in the device to minimize logic required by memory systems to perform refresh control.

Features

- One chip solution to produce RFCK timing for the DP8408A, DP8409A, DP8417, DP8418, DP8419, DP8428, DP8429 dynamic RAM controllers
- Programmable refresh clock timer allows for a maximum refresh period with most system clocks
- Timing is completely synchronous with the input clock, preventing race conditions present in some memory controllers
- Includes a refresh request output, simplifying the design of refresh logic in discrete controllers

Connection & Block Diagrams

Dual-In-Line Package



Top View

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Order Number DP84300N
See NS Package Number N24C

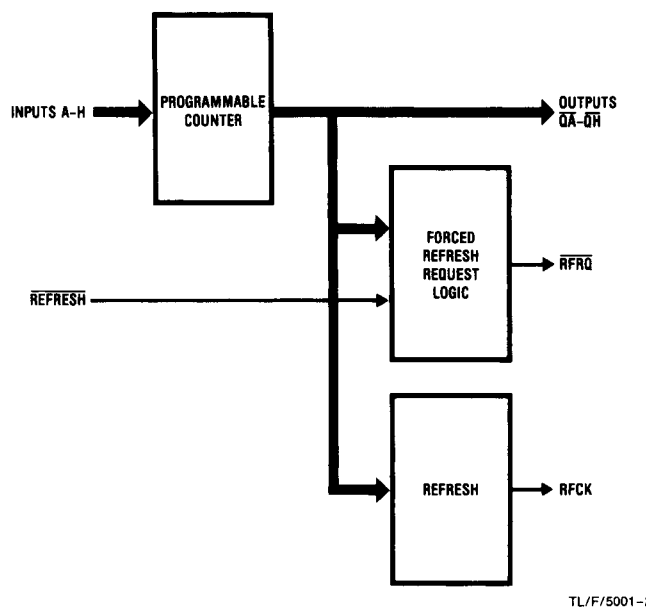

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FIGURE 1

Recommended Operating Conditions (Commercial)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	Min	Typ	Max	Units
V_{CC}, Supply Voltage	4.75	5.00	5.25	V
I_{OH}, High Level Output Current			−3.2	mA
I_{OL}, Low Level Output Current			16	mA
T_A, Operating Free Air Temperature	0		75	°C

Electrical Characteristics over recommended operating temperature range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = Max			0.5	V
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_O = 2.4V, V_{IL} = 0.8V			100	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_O = 0.4V, V_{IL} = 0.8V			−100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−250	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max		150	180	mA

DP84300 Switching Characteristics over recommended ranges of temperature and V_{CC}

Symbol	Parameter		Conditions R_L = 667Ω	Commercial T_A = 0°C to +75°C V_{CC} = 5.0V ±5%			Units
				Min	Typ	Max	
t_{PD}	Clock to Output		C_L = 45 pF		35	50	ns
t_{PZX}	Pin 13 to Output Enable				20	35	ns
t_{PXZ}	Pin 13 to Output Disable		C_L = 5 pF		20	35	ns
t_{PZX}	Input to Output Enable		C_L = 45 pF		35	45	ns
t_{PXZ}	Input to Output Disable		C_L = 5 pF		35	45	ns
t_W	Width of Clock	High		25			ns
		Low		35			ns
t_{SU}	Set-Up Time			50			ns
t_H	Hold Time			0	−15		ns
f_{MAX}	Maximum Frequency			12.5			MHz

Mnemonic Description

INPUT SIGNALS

CLOCK — Provides a time base for the programmable divider.

A-H — Program inputs A through H. These inputs select the number of clock cycles that will produce one refresh period. These inputs are binary encoded, with input A the LSB, and H the MSB. Additionally, all zeros produce the maximum count of 256, and an input of one will reset the counter to one.

$\overline{\text{REFRESH}}$ — This input is used to reset the refresh request output ($\overline{\text{RFRQ}}$).

$\overline{\text{OE}}$ — Output enable. Places the outputs in TRI-STATE®.

$\overline{\text{CE}}$ — Counter enable. This input, when low, enables the timer clock and, when high, stalls the timer.

OUTPUT SIGNALS

$\overline{\text{QA}}$-$\overline{\text{QH}}$ — Refresh timer outputs $\overline{\text{QA}}$ through $\overline{\text{QH}}$. Timer starts at programmed input and counts down to one.

$\overline{\text{RFRQ}}$ — Refresh request. This output goes low on the rising edge of the refresh clock (RFCK). The first input clock edge after the $\overline{\text{REFRESH}}$ input is set low clears this output.

RFCK — Refresh clock. The period of the clock is determined by setting conditions on input pins A through H. This output is low for 20 clocks, and high for the remainder of the period.

Functional Description

The DP84300 block diagram is shown in *Figure 1*. This circuit is basically an 8-bit programmable counter. The user selects the number of input clock cycles required per refresh period and sets the binary equivalent on inputs A through H. A signal of that period is produced at the refresh clock (RFCK) output. This output stays low for 20 clock cycles, and goes high for the balance of the period.

When used with the DP8409A dynamic RAM controller, this duty cycle allows the DP8409A the maximum probability to perform a hidden refresh, while still allowing ample time for the DP8409A to perform a forced refresh when needed.

An additional output is provided to ease the design of systems that don't use the DP8409A. This output is called refresh request ($\overline{\text{RFRQ}}$). Refresh request becomes true at the rising edge of refresh clock, and becomes false on the first rising edge of the input clock after a refresh.

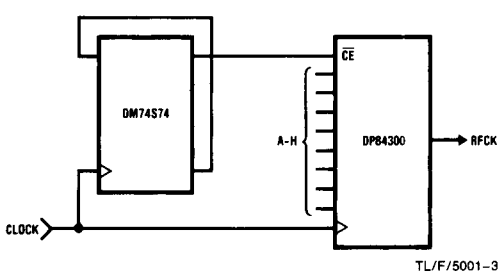
In systems where a divisor of more than 256 is needed, an expansion input ($\overline{\text{CE}}$) has been provided. When this input is high, all counter-related timing is suspended. This excluded actions due to the $\overline{\text{REFRESH}}$ input. The circuits in *Figures 2a* and *2b* show how to expand the range of the timer by 2x or by up to 4096 clock cycles. *Figures 3a* and *3b* show two typical applications using the DP84300.

By using the clock enable input, it is also possible to change the duty cycle of the refresh clock. The circuits in *Figures 4a* and *4b* show how this may be done.

To reset the counter to a known state, select an input divisor of one. On the next clock edge the counter will reset to one. On the next clock edge whatever input divisor that is present on input A-H will be loaded into the counters.

TABLE I. Divider Constants for Generation of a 15.5 μs Clock

CPU Clock Frequency	Divisor Input	Actual Period of Output	% Chance of Hidden Refresh
2 MHz	31	15.5 μs	35%
3 MHz	46	15.3 μs	56%
4 MHz	62	15.5 μs	67%
5 MHz	77	15.6 μs	74%
6 MHz	93	15.5 μs	78%
7 MHz	109	15.6 μs	81%
8 MHz	124	15.5 μs	83%
9 MHz	140	15.6 μs	85%
10 MHz	155	15.5 μs	87%



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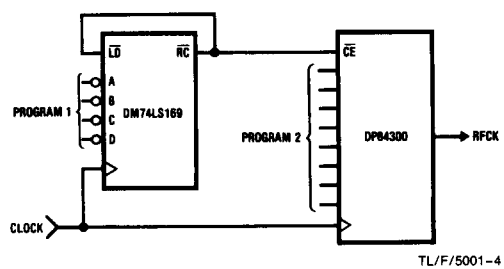
Period of RFCK = 2x program input

FIGURE 2a. Expansion of Clock Divisor by 2x



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Period of RFCK 2 = program A × program B

$\overline{\text{RFCK}}$ is low for 20x program 1 clocks

Maximum period of RFCK is 4096 clocks

FIGURE 2b. Typical Expansion for the DP84300

Functional Description (Continued)

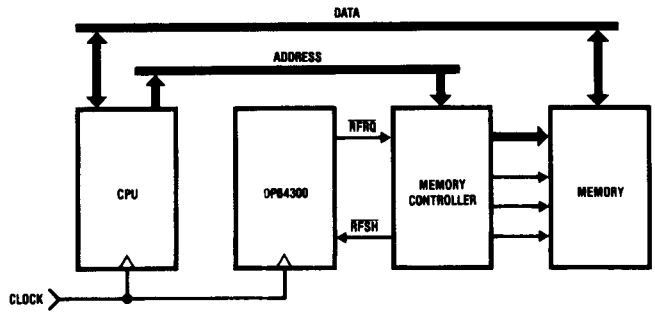

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FIGURE 3a. Dynamic Memory System Using DP84300

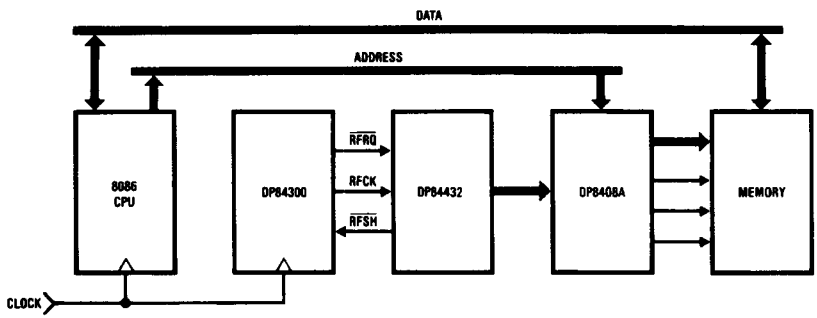

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FIGURE 3b. 8086 System Using Dynamic RAMs DP8408A, DP84300, and DP84432

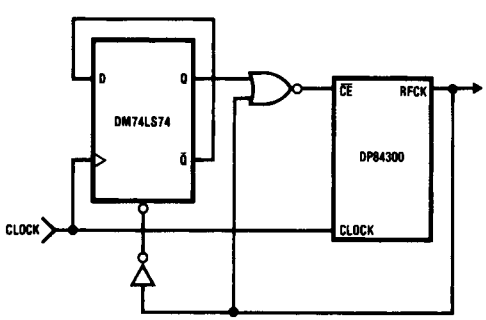

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FIGURE 4a. Circuit for Extending RFCK Low to 40 Clocks

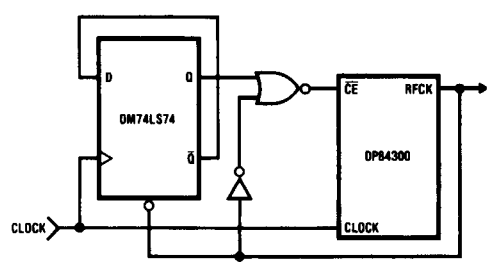

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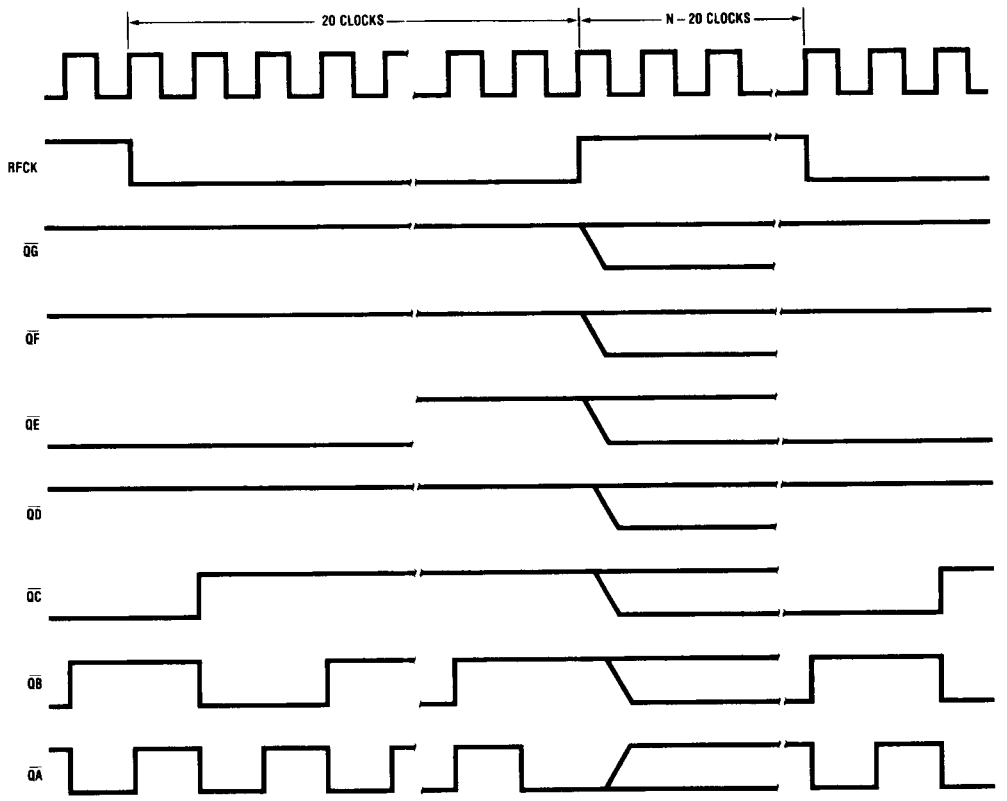
FIGURE 4b. Circuit for Extending RFCK High by 2x

Timing Diagrams

Refresh Timer Outputs



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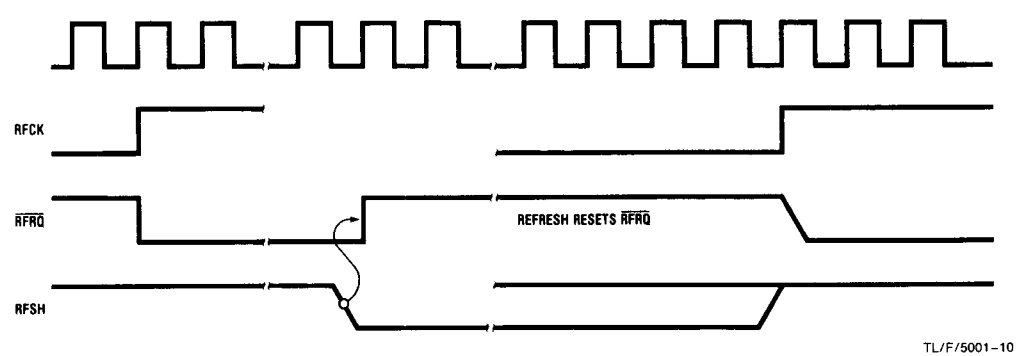
$\overline{\text{REFRESH REQUEST}}$ ($\overline{\text{RFRQ}}$) Output Timing



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