Micro Power Systems

MP7524

CMOS
Buffered Multiplying 8-Bit
Digital-to-Analog Converter

FEATURES

- **Full Four-Quadrant Multiplication**
- **On-chip Bus Interface Logic**
- **+5 V to +15 V Operation**
- **Low Power Consumption**
- **Monotonicity Guranteed (Full Temperature Range)**
- **PDIP, CDIP, SOIC & PLCC Packages Available**

APPLICATIONS

- **Microprocessor Controlled Gain Circuits**
- **Microprocessor Controlled Attenuator Circuits**
- **Microprocessor Controlled Function Generation**
- **Precision AGC Circuits**
- **Bus Structured Instruments**

GENERAL DESCRIPTION

The MP7524 is a low cost, 8-bit monolithic CMOS D/A Converter designed for direct interface to most microprocessors.

Basically an 8-bit DAC with input latches, the MP7524's load cycle is similar to the "write" cycle of a random access memory. Using an advanced thin-film on CMOS fabrication process, the MP7524 provides accuracy to 1/8 LSB with power dissipation of only 10mW.

Featuring operation from +5 V to +15 V, the MP7524 interfaces directly to most microprocessor buses or output ports. Excellent multiplying characteristics (2- or 4-quadrant) make the MP7524 an ideal choice for many microprocessor controlled gain setting and signal control applications.

Specified for operation over the commercial / industrial (–40 to +85°C) and military (–55 to +125°C) temperature ranges, the MP7524 is available in Plastic and Ceramic dual-in-line, Surface Mount (SOIC) and Plastic Leaded Chip Carrier (PLCC) packages.

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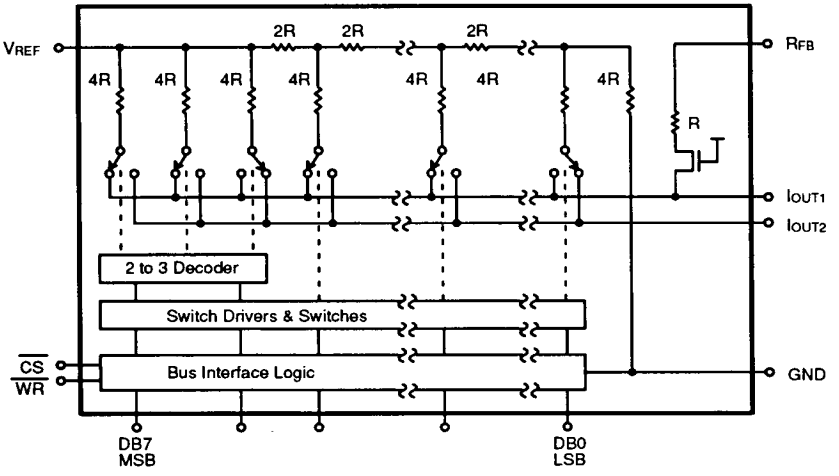
SIMPLIFIED BLOCK DIAGRAM

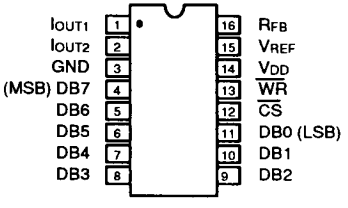


3 Segment D/A Converter with Termination to GND
Logical "1" at Digital Input Steers Current to I_{OUT1}

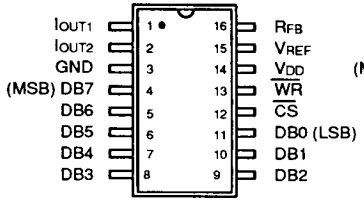
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	Relative Accuracy	Differential Non-Linearity	Gain Error
Plastic Dip	–40 to +85°C	MP7524JN	±1/2 LSB	±1 LSB	±0.6% FSR
Plastic Dip	–40 to +85°C	MP7524KN	±1/4 LSB	±1 LSB	±0.6% FSR
Plastic Dip	–40 to +85°C	MP7524LN	±1/8 LSB	±1 LSB	±0.6% FSR
SOIC (Narrow)	–40 to +85°C	MP7524JR	±1/2 LSB	±1 LSB	±0.6% FSR
SOIC (Narrow)	–40 to +85°C	MP7524KR	±1/4 LSB	±1 LSB	±0.6% FSR
SOIC (Wide)	–40 to +85°C	MP7524JS	±1/2 LSB	±1 LSB	±0.6% FSR
SOIC (Wide)	–40 to +85°C	MP7524KS	±1/4 LSB	±1 LSB	±0.6% FSR
SOIC (Wide)	–40 to +85°C	MP7524LS	±1/8 LSB	±1 LSB	±0.6% FSR
PLCC	–40 to +85°C	MP7524JP	±1/2 LSB	±1 LSB	±0.6% FSR
PLCC	–40 to +85°C	MP7524KP	±1/4 LSB	±1 LSB	±0.6% FSR
PLCC	–40 to +85°C	MP7524LP	±1/8 LSB	±1 LSB	±0.6% FSR
Ceramic Dip	–40 to +85°C	MP7524AD	±1/2 LSB	±1 LSB	±0.6% FSR
Ceramic Dip	–40 to +85°C	MP7524BD	±1/4 LSB	±1 LSB	±0.6% FSR
Ceramic Dip	–40 to +85°C	MP7524CD	±1/8 LSB	±1 LSB	±0.6% FSR
Ceramic Dip	–55 to +125°C	MP7524SD	±1/2 LSB	±1 LSB	±0.6% FSR
Ceramic Dip	–55 to +125°C	MP7524SD/883	±1/2 LSB	±1 LSB	±0.6% FSR
Ceramic Dip	–55 to +125°C	MP7524TD	±1/4 LSB	±1 LSB	±0.6% FSR
Ceramic Dip	–55 to +125°C	MP7524TD/883	±1/4 LSB	±1 LSB	±0.6% FSR
Ceramic Dip	–55 to +125°C	MP7524UD	±1/8 LSB	±1 LSB	±0.6% FSR
Ceramic Dip	–55 to +125°C	MP7524UD/883	±1/8 LSB	±1 LSB	±0.6% FSR

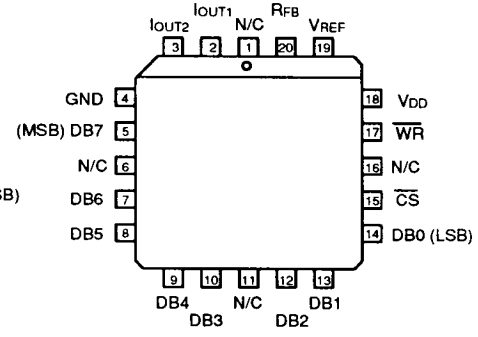
PIN CONFIGURATIONS



16 Pin CDIP, PDIP (0.300")



16 Pin SOIC
(Jedec, 0.150" & 0.300")



20 Pin PLCC (0.350")

PIN OUT DEFINITIONS

CDIP, PDIP and SOIC

PIN NO.	NAME	DESCRIPTION
1	I_{OUT1}	Current Output 1
2	I_{OUT2}	Current Output 2
3	GND	Ground
4	DB7	Data Bit 7 (MSB)
5	DB6	Data Bit 6
6	DB5	Data Bit 5
7	DB4	Data Bit 4
8	DB3	Data Bit 3
9	DB2	Data Bit 2
10	DB1	Data Bit 1
11	DB0	Data Bit 0 (LSB)
12	$\overline{CS}$	Chip Select
13	$\overline{WR}$	Write
14	V_{DD}	Power Supply
15	V_{REF}	Reference Input
16	R_{FB}	Feedback Resistance

PLCC

PIN NO.	NAME	DESCRIPTION
1	N/C	No Connection
2	I_{OUT1}	Current Output 1
3	I_{OUT2}	Current Output 2
4	GND	Ground
5	DB7	Data Bit 7 (MSB)
6	N/C	No Connection
7	DB6	Data Bit 6
8	DB5	Data Bit 5
9	DB4	Data Bit 4
10	DB3	Data Bit 3
11	N/C	No Connection
12	DB2	Data Bit 2
13	DB1	Data Bit 1
14	DB0	Data Bit 0 (LSB)
15	$\overline{CS}$	Chip Select
16	N/C	No Connection
17	$\overline{WR}$	Write
18	V_{DD}	Power Supply
19	V_{REF}	Reference Input
20	R_{FB}	Feedback Resistance

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 5 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE (1)								FSR = Full Scale Range
Resolution (All Grades)	N	8			8		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
J, A, S				±1/2		±1/2		
K, B, T				±1/2		±1/2		
L, C, U				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
J, A, S				±1		±1		
K, B, T				±1		±1		
L, C, U				±1		±1		
Gain Error	GE			±1.0		±1.4	% FSR	Using Internal R_{FB} Digital Inputs = V_{INH}
Power Supply Rejection Ratio	PSRR			800		1600	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 10% Digital Inputs = V_{INH}
Output Leakage Current (Pin 1)	I_{OUT1}			±50nA		±400nA	nA	Digital Inputs = V_{INL}
Output Leakage Current (Pin 2)	I_{OUT2}			±50nA		±400nA	nA	Digital Inputs = V_{INH}
DYNAMIC PERFORMANCE								RL = 100Ω, C_L = 10pF
Current Settling Time (2)	ts			100		150	ns	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT1} (2)	FT			±1/2		±1	LSB	V_{REF}=100KHz, 20 Vp-p, sinewave
at I_{OUT2}				±1/2		±1	LSB	DB0-DB7 = 0 V, $\overline{CS}$ = $\overline{WR}$ = 0 V
REFERENCE INPUT								
Input Resistance	R_{IN}	5		20	5	20	KΩ	
DIGITAL INPUTS (3)								
Logical "1" Voltage	V_{IH}	+2.4			+2.4		V	
Logical "0" Voltage	V_{IL}			+0.8		+0.8	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	
Input Capacitance (2)	C_{IN}			20		20	pF	V_{IN} = 0 V
ANALOG OUTPUTS (2)								
Output Capacitance								
	C_{OUT1}			70		70	pF	DAC Inputs all 1's
	C_{OUT1}			30		30	pF	DAC Inputs all 0's
	C_{OUT2}			20		20	pF	DAC Inputs all 1's
	C_{OUT2}			60		60	pF	DAC Inputs all 0's
POWER SUPPLY (5)								
Supply Current	I_{DD}		1	2		2	mA	All digital inputs = 0 V or all = 5 V
			1	2		2	mA	All digital inputs = V_{IL} or all = V_{IH}

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
SWITCHING CHARACTERISTICS (2, 4)								
Chip Select to Write Set-Up Time	t_{CS}						ns	
J, K, L, A, B, C		170			220			
S, T, U		170			240			
Chip Select to Write Hold Time	t_{CH}	0			0		ns	
Data Valid to Write Set-Up Time	t_{DS}	135			170		ns	
Data Valid to Write Hold Time	t_{DH}	10			10		ns	
Write Pulse Width	t_{WR}						ns	
J, K, L, A, B, C		170			220			
S, T, U		170			240			

NOTES:

(1) Full Scale Range (FSR) is 10V for unipolar mode and ±10V for bipolar.
(2) Guaranteed but not production tested .
(3) Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
(4) See timing diagram.
(5) Specified values guarantee functionality. Refer to other parameters for accuracy.

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Specifications are subject to change without notice

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE (1)								FSR = Full Scale Range
Resolution (All Grades)	N	8			8		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
J, A, S				±1/2		±1/2		
K, B, T				±1/4		±1/4		
L, C, U				±1/8		±1/8		
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
J, A, S				±1		±1		
K, B, T				±1		±1		
L, C, U				±1		±1		
Gain Error	GE			±0.5		±0.6	% FSR	Using Internal R_{FB} Digital Inputs = V_{INH}
Power Supply Rejection Ratio	PSRR			200		400	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 10% Digital Inputs = V_{INH}
Output Leakage Current (Pin 1)	I_{OUT1}			±50nA		±200nA	nA	Digital Inputs = V_{INL}
Output Leakage Current (Pin 2)	I_{OUT2}			±50nA		±200nA	nA	Digital Inputs = V_{INH}
DYNAMIC PERFORMANCE								RL=100Ω, CL=13pF
Current Settling Time (2)	ts			50		100	ns	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT1} (2)	FT			±0.50		±1.00	LSB	V_{REF} = 10KHz, 20 Vp-p, sinewave
at I_{OUT2}				±0.50		±1.00	LSB	DB0 - DB7 = 0 V, $\overline{CS}$ = $\overline{WR}$ = 0 V
REFERENCE INPUT								
Input Resistance	R_{IN}	5		20	5	20	KΩ	
DIGITAL INPUTS (3)								
Logical "1" Voltage	V_{IH}	+13.5			+13.5		V	
Logical "0" Voltage	V_{IL}			+1.5		+1.5	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	
Input Capacitance (2)	C_{IN}			20		20	pF	
ANALOG OUTPUTS (2)								
Output Capacitance								
	C_{OUT1}			70		70	pF	DAC Inputs all 1's
	C_{OUT1}			30		30	pF	DAC Inputs all 0's
	C_{OUT2}			20		20	pF	DAC Inputs all 1's
	C_{OUT2}			60		60	pF	DAC Inputs all 0's
POWER SUPPLY								
Supply Current	I_{DD}		1	2		2	mA	All digital inputs = 0 V or all = 15 V
			1	2		2	mA	All digital inputs = V_{IL} or all = V_{IH}

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
SWITCHING CHARACTERISTICS (2, 4)								
Chip Select to Write Set-Up Time	t_{CS}						ns	
J, K, L, A, B, C		100			130			
S, T, U		100			150			
Chip Select to Write Hold Time	t_{CH}	0			0		ns	
Data Valid to Write Set-Up Time	t_{DS}						ns	
J, K, L, A, B, C		60			80			
S, T, U		60			100			
Data Valid to Write Hold Time	t_{DH}	10			10		ns	
Write Pulse Width	t_{WR}						ns	
J, K, L, A, B, C		100			130			
S, T, U		100			150			

NOTES:

(1) Full Scale Range (FSR) is 10V for unipolar mode and ±10V for bipolar.
(2) Guaranteed but not production tested.
(3) Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
(4) See timing diagram.
(5) Specified values guarantee functionality. Refer to other parameters for accuracy.

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Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (1, 2) (T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... –0.5, +17 V
Digital Input Voltage to GND (2) .. GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... –0.5 to 7 V
V_{REF} to GND ..... ±25 V
V_{RFB} to GND ..... ±25 V

Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 70°C
CDIP, PDIP, SOIC, PLCC 450mW
Derates above 70°C ..... 6mW/°C

NOTES:

(1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
(2) Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

APPLICATION NOTES

Refer to Applications Section for Additional Information

INTERFACE LOGIC INFORMATION

Mode Selection

MP7524 mode selection is controlled by the $\overline{CS}$ and $\overline{WR}$ inputs.

$\overline{CS}$	$\overline{WR}$	Mode	DAC Response
L	L	Write	DAC responds to data bus (DB0-DB7) inputs
H	X	Hold	Data Bus (DB0-DB7) is locked out
X	H	Hold	DAC holds last data present when $\overline{WR}$ assumed HIGH state

L = LOW state, H = HIGH state, X = Don't care state

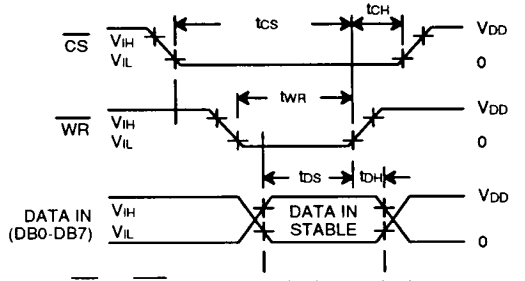
Table 1. Mode Selection Table

Write Mode

When $\overline{CS}$ and $\overline{WR}$ are both LOW, the MP7524 is in the WRITE mode, and the MP7524 analog circuit responds to data activity at the DB0-DB7 data bus inputs. In this mode, the MP7524 acts like a non-latched input D/A converter.

Hold Mode

When either $\overline{CS}$ or $\overline{WR}$ is HIGH, the MP7524 is in the HOLD mode. The MP7524 analog output holds the value corresponding to the last digital input present at DB0-DB7 prior to $\overline{WR}$ or $\overline{CS}$ assuming the high state.



NOTE: If $\overline{CS}$ and $\overline{WR}$ are exercised simultaneously, the t_{DH} specification (as shown in specification table) must be increased by 60 ns.

Figure 1. Write Cycle Timing Diagram

MICROPROCESSOR INTERFACE

MP7524/8080A Interface

Figure 2. shows the MP7524 used in the MCS-80 microcomputer system as a Memory Mapped Output Device. The basic CPU group consists of the 8080A CPU, 8224 clock generator and 8228 system controller/bus driver. The MP7524 $\overline{WR}$ input is connected to the 8228 system data bus outputs. The $\overline{CS}$ input is connected to the system address decoding logic. Note that pull-up resistors R3 and R4 are required to ensure that the $\overline{CS}$ and $\overline{WR}$ input HIGH states reach 3.0V min. Pull-ups are not required on the system data bus since the 8228 VOH is 3.6 V min for DB0-DB7.

System timing is shown in *Figure 3.* Data is loaded into the MP7524 when the $\overline{WR}$ and $\overline{CS}$ inputs are both LOW. The data is latched into the MP7524 when $\overline{WR}$ returns HIGH. MP7524 updating is accomplished by using any of the 8080A memory write instructions (such as MOV M, r).

The MP7524 can also be addressed and loaded as an isolated Output Device by connecting the MP7524 $\overline{WR}$ input to the 8228 $\overline{I/O\ W}$ terminal (instead of $\overline{MEMW}$).

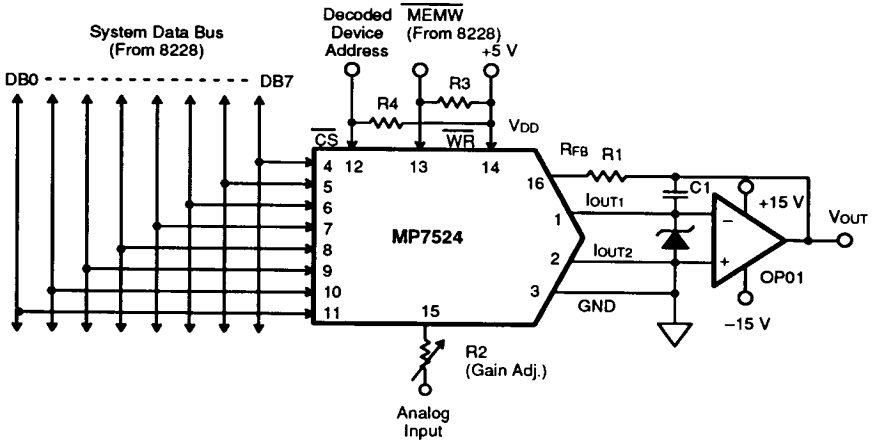


Figure 2. MP7524/8080A Interface

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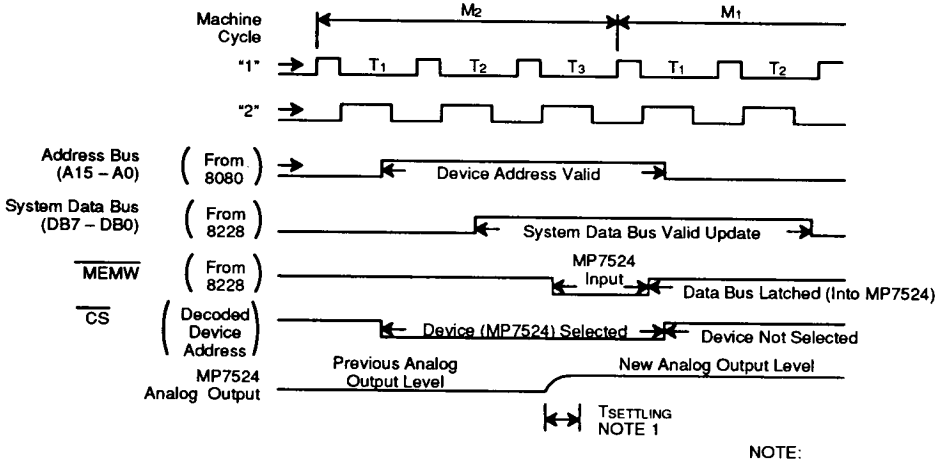

NOTE:
1. Settling Time Is Dependent Primarily Upon Output Amplifier Slewing And Settling Characteristics. Waveform Shown Is Not Representative Of Any Specific Amplifier

Figure 3. Timing Diagram