OKI semiconductor

MSM80C154/MSM83C154

CMOS 8-bit One-Chip Microcontroller

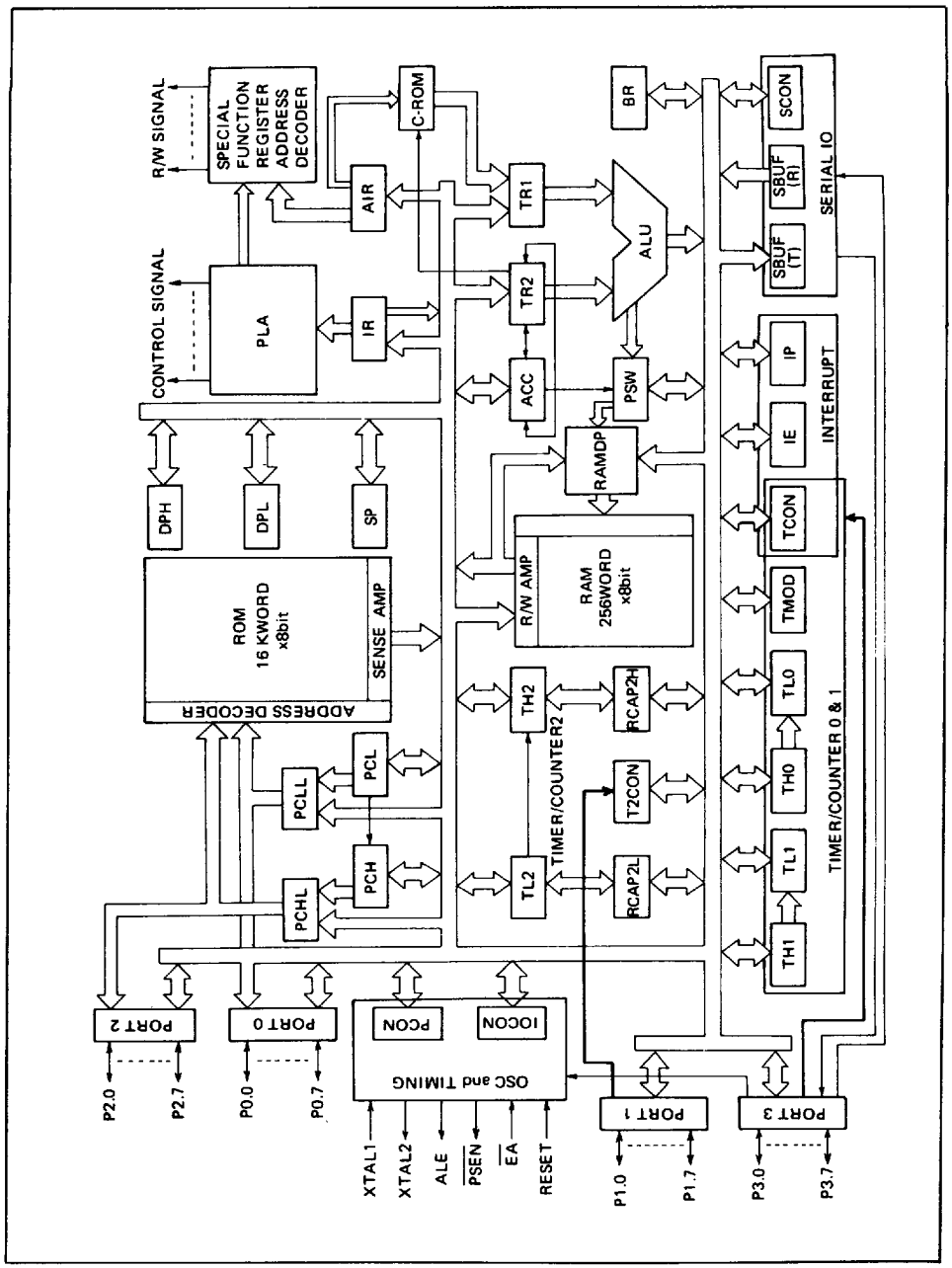
GENERAL DESCRIPTION

The MSM83C154/MSM80C154 is a high performance 8-bit one-chip microcontroller implementing large integration, high speed and low power consumption by 2 μm silicon gate CMOS process technology.
The MSM83C154 features 16K byte ROM, 256 byte RAM, 32 I/O ports, three 16-bit timer/counters, multifunctional serial port and clock generator. In addition, the MSM83C154 has three standby modes enabling further power reduction.
The MSM80C154 is identical to the MSM83C154 except the omission of 16K byte ROM.

FEATURES

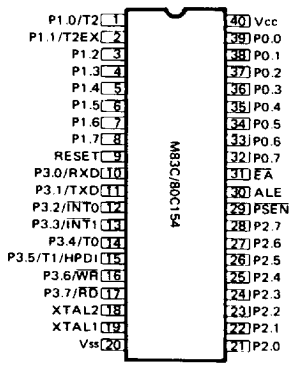
- Fully static circuit
- On-chip program memory : 16K x 8 bit ROM (MSM83C154 only)
- On-chip data memory : 256 x 8 bit RAM
- External program memory address space : 64K bytes
- External data memory address space : 64K bytes
- I/O ports
  (Port 1, 2, 3, impedance programmable) : 32
- 16-bit timer/counters
  (includes watch dog timer & 32 bit timer) : 3
- Multifunctional serial port : I/O Expansion mode
  : UART mode (featuring error detection)
- 6-source 2-priority level interrupt and multi-level interrupt available by programming IP and IE registers
- Memory-mapped special function registers
- Bit addressable data memory and SFRs
- Minimum instruction cycle : 1.0μs @ 12 MHz operation (MSM80C154/MSM83C154)
  : 0.75μs @ 16 MHz operation (MSM80C154-1/MSM83C154-1)
- "Multiply"/"divide" instruction cycle : 3 μs @16 MHz operation
- Standby functions : Idle mode (CPU halt)
  : Power down mode (Oscillator stop)
  Activated by Software or Hardware; Providing ports with floating or active status
  The software power down mode is terminated by interrupt signal enabling execution from the interrupted address.
- Lower power consumption achieved by 2 μm silicon gate CMOS process
- Upward compatible with MSM80C51/80C31
- Packages : 40 pin plastic DIP (DIP40-P-600)
  44 pin plastic QFP (QFP44-P-910-K)
  44 pin plastic QFP (QFP44-P-910-VIK)
  44 pin PLCC (QFJ44-P-S650)

CIRCUIT BLOCK DIAGRAM

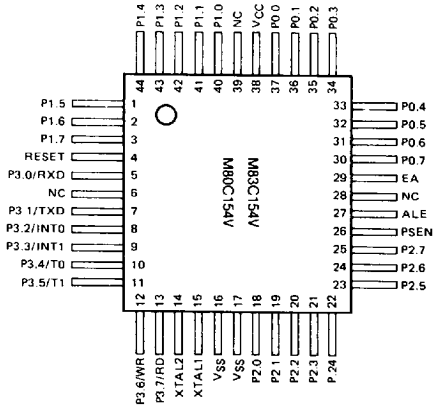


PIN CONFIGURATION

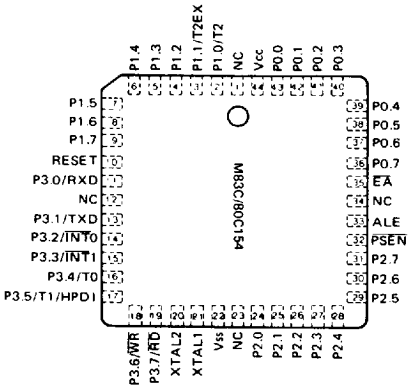
MSM83C154-XXRS/MSM80C154RS
(Top-View) 40 Lead Plastic DIP



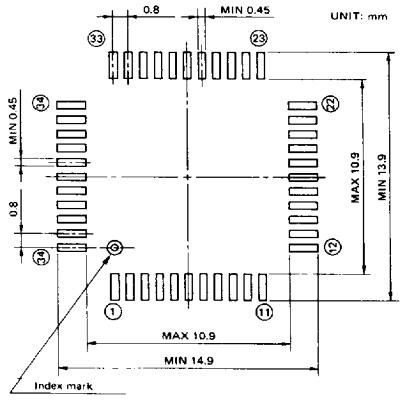
MSM83C154V-XXGS/MSM80C154VGS
(Top-View) 44 Lead Plastic Package



MSM83C154-XXJS/MSM80C154JS *1
(Top-View) 44 Lead Plastic Leaded Chip Carrier



RECOMMENDED FOOTPRINT
FOR QPD PACKAGE



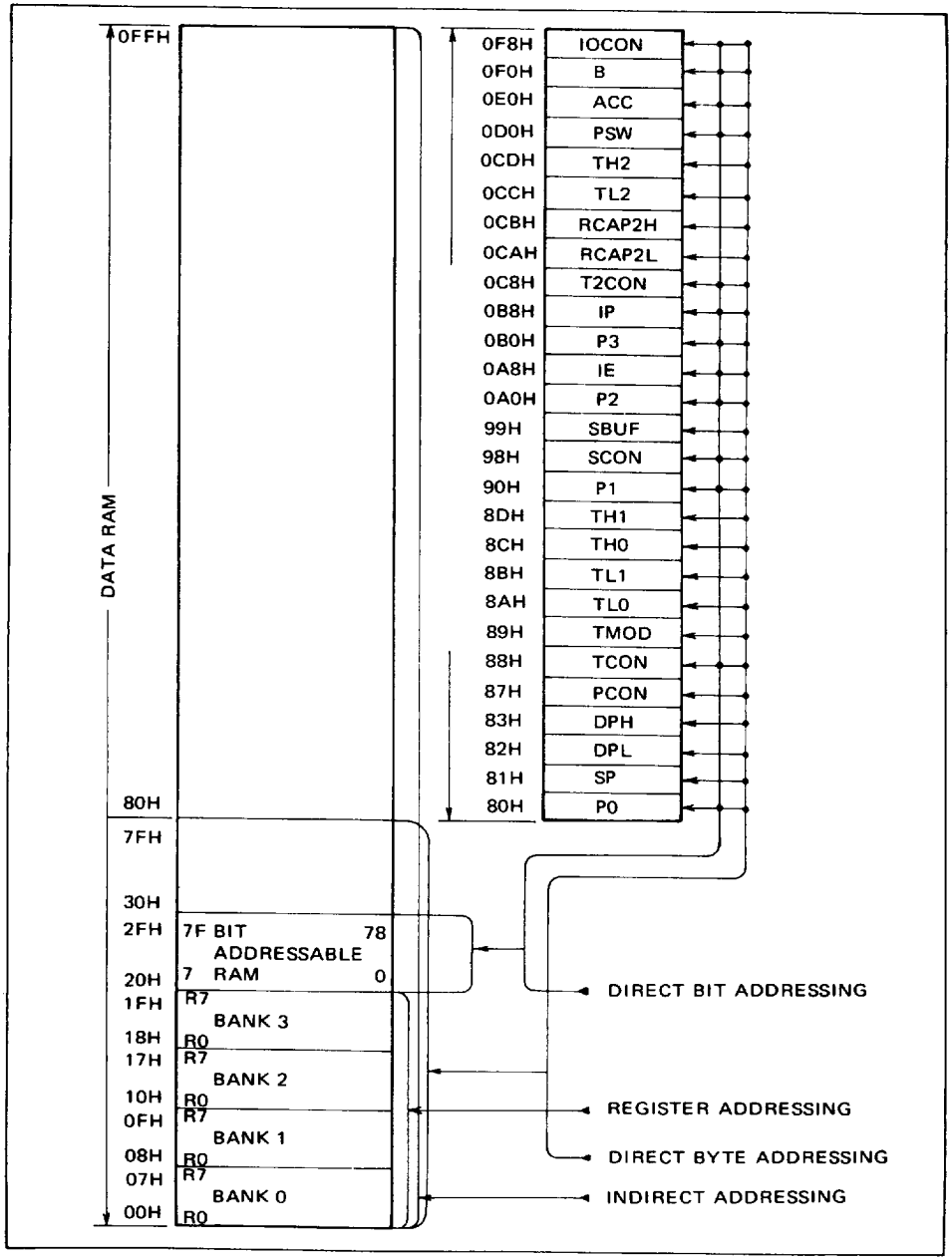
PIN FUNCTIONS

Pin Name	Description
P0.0 ~ P0.7	Bidirectional I/O ports. They are also the data/address bus (input/output of data and output of lower 8-bit address when external memory is accessed). They are open drain output when used as I/O ports, but tri-state output when used as data/address bus.
P1.0 ~ P1.7	P1.0 to P1.7 are quasi-bidirectional I/O ports. They are pulled up internally when used as input ports. Two of them have the following secondary functions: • P1.0 (T2) : Used as external clock input pin for the timer/counter 2. • P1.1 (T2EX) : Used as trigger input for the timer/counter 2 to be reloaded or captured; causing the timer/counter 2 interrput.

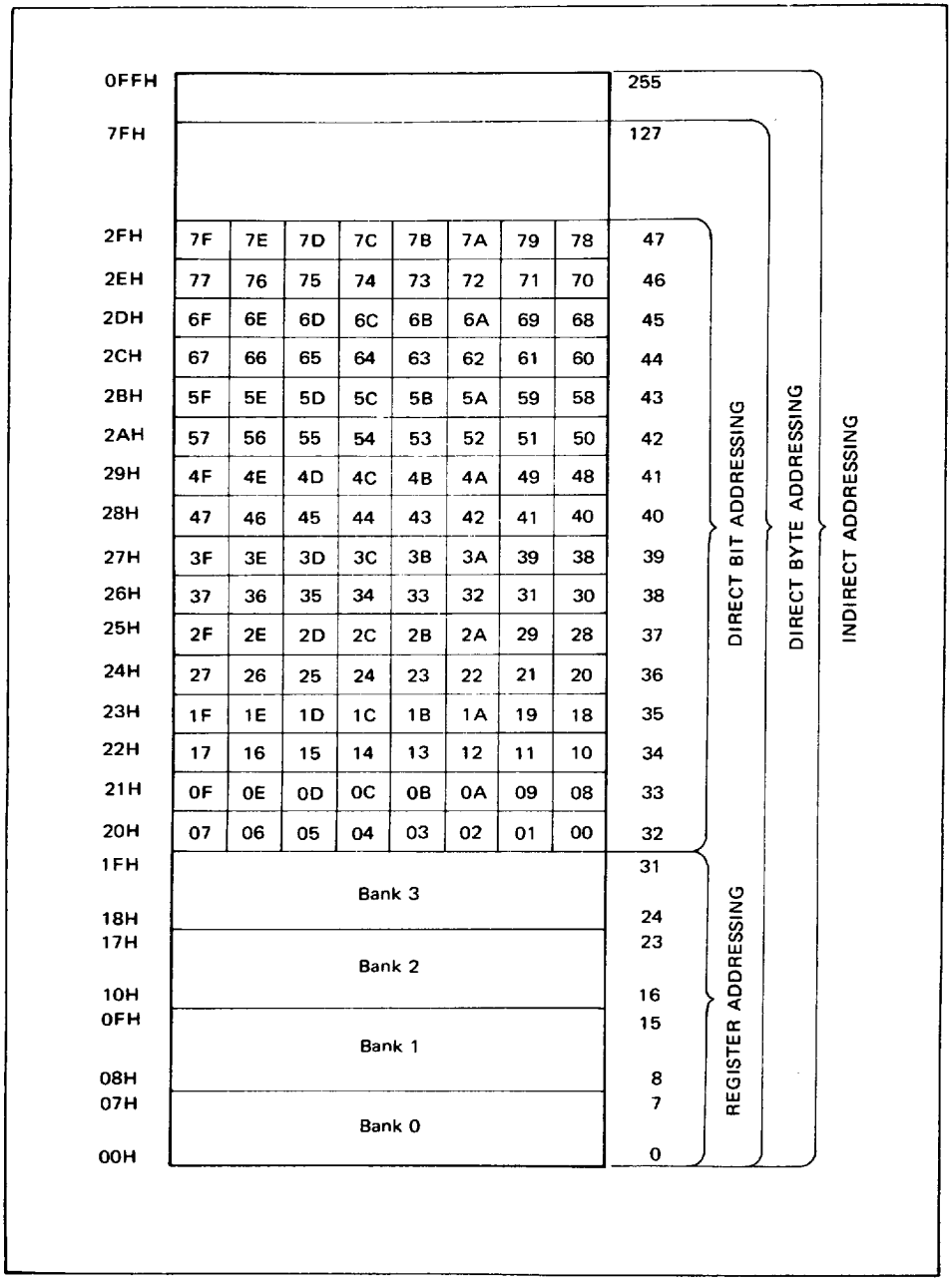
PIN FUNCTIONS (CONT.)

Pin Name	Description
P2.0 ~ P2.7	P2.0 to P2.7 are quasi-bidirectional I/O ports. They also output the higher 8-bit address when an external memory is accessed. They are pulled up internally when used as input ports.
P3.0 ~ P3.7	P3.0 to P3.7 are quasi-bidirectional I/O ports. They are pulled up internally when used as input ports. They also have the following secondary functions: • P3.0 (RXD) Serial data input/output in the I/O expansion mode and serial data input in the UART mode when the serial port is used. • P3.1 (TXD) Synchronous clock output in the I/O expansion mode and serial data output in the UART mode when the serial port is used. • P3.2 ($\overline{INT0}$) Used as input pin for the external interrupt 0, and as count-up control pin for the timer/counter 0. • P3.3 ($\overline{INT1}$) Used as input pin for the external interrupt 1, and as count-up control pin for the timer/counter 1. • P3.4 (T0) Used as external clock input pin for the timer/counter 0. • P3.5 (T1) Used as external clock input pin for the timer/counter 1 and power down mode control input pin. • P3.6 ($\overline{WR}$) Output of the write strobe signal when data is written into external data memory. • P3.7 ($\overline{RD}$) Output of the read strobe signal when data is read from external data memory.
ALE	Address latch enable output for latching the lower 8-bit address during external memory access. Two ALE pulses are activated per machine cycle except during external data memory access at which time one ALE pulse is skipped.
$\overline{PSEN}$	Program store enable output which enable the external memory output to the bus during external program memory access. Two $\overline{PSEN}$ pulses are activated per machine cycle except during external data memory access at which two $\overline{PSEN}$ pulses are skipped.
$\overline{EA}$	When $\overline{EA}$ is held at "H" level, the MSM83C154 executes instructions from internal program memory at address 0000H to 3FFFH, and executes instructions from external program memory above address 3FFFH. When $\overline{EA}$ is held at "L" level, the MSM80C154/MSM83C154 executes instructions from external program memory for all addresses.
RESET	If this pin remains "H" for at least 1 μ second, the MSM80C154/MSM83C154 is reset. Since this pin is pulled down internally, a power-on reset is achieved by simply connecting a capacitor between Vcc and this pin.
XTAL1	Oscillator inverter input pin. External clock is input through XTAL1 pin.
XTAL2	Oscillator inverter output pin.
V_{CC}	Power supply pin during both normal operation and standby operations.
V_{SS}	GND pin.

DATA MEMORY AND SPECIAL FUNCTION REGISTER LAYOUT DIAGRAM



DETAILED DIAGRAM OF DATA MEMORY (RAM)



DETAILED DIAGRAM OF SPECIAL FUNCTION REGISTERS

Direct Byte Address	Bit Address (MSB)							(LSB)	Special Function Register Symbol
	WDT	T32	SERR	IZC	P3HZ	P2HZ	P1HZ	ALF	
0F8H	FF	FE	FD	FC	FB	FA	F9	F8	IOCON
0F0H	F7	F6	F5	F4	F3	F2	F1	F0	B
0E0H	E7	E6	E5	E4	E3	E2	E1	E0	ACC
	CY	AC	F0	RS1	RS0	0V	F1	P	
0D0H	D7	D6	D5	D4	D3	D2	D1	D0	PSW
0CDH	Not Bit Addressable								TH2
0CCH	Not Bit Addressable								TL2
0CBH	Not Bit Addressable								RCAP2H
0CAH	Not Bit Addressable								RCAP2L
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	
0C8H	CF	CE	CD	CC	CB	CA	C9	C8	T2CON
	PCT		PT2	PS	PT1	PX1	PT0	PX0	
0B8H	BF	–	BD	BC	BB	BA	B9	B8	IP
0B0H	B7	B6	B5	B4	B3	B2	B1	B0	P3
	EA		ET2	ES	ET1	EX1	ET0	EX0	
0A8H	AF	–	AD	AC	AB	AA	A9	A8	IE
0A0H	A7	A6	A5	A4	A3	A2	A1	A0	P2
99H	Not Bit Addressable								SBUF
	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	
98H	9F	9E	9D	9C	9B	9A	99	98	SCON
90H	97	96	95	94	93	92	91	90	P1

Direct Byte Address	Bit Address (MSB)							(LSB)	Special Function Register Symbol
8DH	Not Bit Addressable								TH1
8CH	Not Bit Addressable								TH0
8BH	Not Bit Addressable								TL1
8AH	Not Bit Addressable								TL0
89H	Not Bit Addressable								TMOD
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	
88H	8F	8E	8D	8C	8B	8A	89	88	TCON
87H	Not Bit Addressable								PCON
83H	Not Bit Addressable								DPH
82H	Not Bit Addressable								DPL
81H	Not Bit Addressable								SP
80H	87	86	85	84	83	82	81	80	P0

SPECIAL FUNCTION REGISTERS

Timer mode register (TMOD)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
TMOD	89H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0

BIT LOCATION	FLAG	FUNCTION		
TMOD.0	M0	M1	M0	Timer/counter 0 mode setting
		0	0	8-bit timer/counter with 5-bit prescalar.
		0	1	16-bit timer/counter.
		1	0	8-bit timer/counter with 8-bit auto reloading.
TMOD.1	M1	1	1	Timer/counter 0 separated into TL0 (8-bit) timer/counter and TH0 (8-bit) timer/counter. TF0 is set by TL0 carry, and TF1 is set by TH0 carry.
TMOD.2	C/$\overline{T}$	Timer/counter 0 count clock designation control bit. XTAL1 · 2 divided by 12 clocks is the input applied to timer/counter 0 when C/$\overline{T}$ = "0". The external clock applied to the T0 pin is the input applied to timer/counter 0 when C/$\overline{T}$ = "1".		
TMOD.3	GATE	When this bit is "0", the TR0 bit of TCON (timer control register) is used to control the start and stop of timer/counter 0 counting. If this bit is "1", timer/counter 0 starts counting when both the TR0 bit of TCON and $\overline{INT0}$ pin input signal are "1", and stops counting when either is changed to "0".		
TMOD.4	M0	M1	M0	Timer/counter 1 mode setting.
		0	0	8-bit timer/counter with 5-bit prescalar.
		0	1	16-bit timer/counter.
		1	0	8-bit timer/counter with 8-bit auto reloading.
TMOD.5	M1	1	1	Timer/counter 1 operation stopped.
TMOD.6	C/$\overline{T}$	Timer/counter 1 count clock designation control bit. XTAL1 · 2 divided by 12 clocks is the input applied to timer/counter 1 when C/$\overline{T}$ = "0". The external clock applied to the T1 pin is the input applied to timer/counter 1 when C/$\overline{T}$ = "1".		
TMOD.7	GATE	When this bit is "0", the TR1 bit of TCON is used to control the start and stop of timer/counter 1 counting. If this bit is "1", timer/counter 1 starts counting when both the TR1 bit of TCON and $\overline{INT1}$ pin input signal are "1", and stops counting when either is changed to "0".		

Power control register (PCON)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
PCON	87H	SMOD	HPD	RPD	–	GF1	GF0	PD	IDL

BIT LOCATION	FLAG	FUNCTION
PCON.0	IDL	IDLE mode set when this bit is set to "1". CPU operations are stopped when IDLE mode is set, but XTAL1·2, timer/counters 0, 1, and 2, the interrupt circuits, and serial port remain active. IDLE mode is cancelled when the CPU is reset or when an interrupt is generated.
PCON.1	PD	PD mode set when this bit is set to "1". CPU operations and XTAL1÷2 are stopped when PD mode is set. PD mode is cancelled when the CPU is reset or when an interrupt is generated.
PCON.2	GF0	General purpose bit. Testing this flag when IDLE mode is cancelled by an interrupt shows whether the interrupt is a normal interrupt or an IDLE mode release interrupt.
PCON.3	GF1	General purpose bit. Testing this flag when PD mode is cancelled by an interrupt shows whether the interrupt is a normal interrupt or a PD mode release interrupt.
PCON.4	–	Reserved bit. The output data is "1" if the bit is read.
PCON.5	RPD	Bit used to specify cancellation of CPU power down mode (IDLE or PD) by interrupt signal. Power down mode cannot be cancelled by interrupt signal if interrupt is not enabled by IE (interrupt enable register) when this bit is "0". If the interrupt flag is set to "1" by an interrupt request signal when this bit is "1" (even if interrupt is disabled), the program is executed from the next address of the power down mode setting instruction. The flag is reset to "0" by software.
PCON.6	HPD	The hard power down setting mode is enabled when this bit is set to "1". If the level of the power failure detect signal applied to the HPDI pin (pin 3.5) is changed from "1" to "0" when this bit is "1", XTAL1·2 oscillation is stopped and the system is put into hard power down mode. HPD mode is cancelled when the CPU is reset.
PCON.7	SMOD	When the timer/counter 1 carry signal is used as a clock in mode 1, 2 or 3 of the serial port, this bit has the following functions. The serial port operation clock is reduced by 1/2 when the bit is "0" for delayed processing. And when the bit is "1", the serial port operation clock is normal for faster processing.

Timer control register (TCON)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
TCON	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

BIT LOCATION	FLAG	FUNCTION
TCON.0	IT0	External interrupt 0 signal used in level detect mode when this bit is "0", and in trigger detect mode when "1".
TCON.1	IE0	Interrupt request flag for external interrupt 0. Bit is reset automatically when interrupt is serviced. Bit can be set and reset by software when IT0 = "1".
TCON.2	IT1	External interrupt 1 signal used in level detect mode when this bit is "0", and in trigger detect mode when "1".
TCON.3	IE1	Interrupt request flag for external interrupt 1. Bit is reset automatically when interrupt is serviced. Bit can be set and reset by software when IT1 = "1".
TCON.4	TR0	Counting start and stop control bit for timer/counter 0. Timer/counter 0 starts counting when this bit is "1", and stops counting when "0".
TCON.5	TF0	Interrupt request flag for timer interrupt 0. Bit is reset automatically when interrupt is serviced. Bit is set to "1" when carry signal is generated from timer/counter 0.
TCON.6	TR1	Counting start and stop control bit for timer/counter 1. Timer/counter 1 starts counting when this bit is "1", and stops counting when "0".
TCON.7	TF1	Interrupt request flag for timer interrupt 1. Bit is reset automatically when interrupt is serviced. Bit is set to "1" when carry signal is generated from timer/counter 1.

Serial port control register (SCON)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
SCON	98H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI

BIT LOCATION	FLAG	FUNCTION
SCON.0	RI	"End of serial port reception" interrupt request flag. This flag must be reset by software during interrupt service routine. This flag is set after the eighth bit of data has been received when in mode 0, or by the STOP bit when in any other mode. In mode 2 or 3, however, RI is not set if the RB8 data is "0" with SM2 = "1". RI is set in mode 1 if STOP bit is received when SM2 = "1".
SCON.1	TI	"End of serial port transmission" interrupt request flag. This flag must be reset by software during interrupt service routine. This flag is set after the eighth bit of data has been sent when in mode 0, or after the last bit of data has been sent when in any other mode.
SCON.2	RB8	The ninth bit of data received in mode 2 or 3 is passed to RB8. The STOP bit is applied to RB8 if SM2 = "0" when in mode 1. RB8 can not be used in mode 0.
SCON.3	TB8	The TB8 data is sent as the ninth data bit when in mode 2 or 3. Any desired data can be set in TB8 by software.
SCON.4	REN	Reception enable control bit No reception when REN = "0". Reception enabled when REN = "1".
SCON.5	SM2	If the ninth bit of received data is "0" with SM2 = "1" in mode 2 or 3, the "end of reception" signal is not set in the RI flag. Nor is the "end of reception" signal set in the RI flag if the STOP bit is not "1" when SM2 = "1" in mode 1.
SCON.6	SM1	
SCON.7	SM0	

SM0	SM1	MODE	
0	0	0	8-bit shift register I/O
0	1	1	8-bit UART variable baud rate
1	0	2	9-bit UART 1/32 XTAL1, 1/64 XTAL1 baud rate
1	1	3	9-bit UART variable baud rate

Interrupt enable register (IE)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
IE	0A8H	EA	–	ET2	ES	ET1	EX1	ET0	EX0

BIT LOCATION	FLAG	FUNCTION
IE.0	EX0	Interrupt control bit for external interrupt 0. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.1	ET0	Interrupt control bit for timer interrupt 0. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.2	EX1	Interrupt control bit for external interrupt 1. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.3	ET1	Interrupt control bit for timer interrupt 1. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.4	ES	Interrupt control bit for serial port. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.5	ET2	Interrupt control bit for timer interrupt 2. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.6	–	Reserved bit. The output data is "1" if the bit is read.
IE.7	EA	Overall interrupt control bit. All interrupts are disabled when bit is "0". All interrupts are controlled by IE.0 thru IE.5 when bit is "1".

Interrupt priority register (IP)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
IP	0B8H	PCT	–	PT2	PS	PT1	PX1	PT0	PX0

BIT LOCATION	FLAG	FUNCTION
IP.0	PX0	Interrupt priority bit for external interrupt 0. Priority is assigned when bit is "1".
IP.1	PT0	Interrupt priority bit for timer interrupt 0. Priority is assigned when bit is "1".
IP.2	PX1	Interrupt priority bit for external interrupt 1. Priority is assigned when bit is "1".
IP.3	PT1	Interrupt priority bit for timer interrupt 1. Priority is assigned when bit is "1".
IP.4	PS	Interrupt priority bit for serial port. Priority is assigned when bit is "1".
IP.5	PT2	Interrupt priority bit for timer interrupt 2. Priority is assigned when bit is "1".
IP.6	–	Reserved bit. The output data is "1" if the bit is read.
IP.7	PCT	Priority interrupt circuit control bit. The priority register contents are valid and priority assigned interrupts can be processed when this bit is "0". When the bit is "1", the priority interrupt circuit is stopped, and interrupts can only be controlled by the interrupt enable register (IE).

Program status word register (PSW)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
PSW	0D0H	CY	AC	F0	RS1	RS0	OV	F1	P

BIT LOCATION	FLAG	FUNCTION
PSW.0	P	Accumulator (ACC) parity indicator. "1" when the "1" bit number in the accumulator is an odd number, and "0" when an even number.
PSW.1	F1	User flag which may be set to "0" or "1" as desired by the user.
PSW.2	OV	Overflow flag which is set if the carry C6 from bit 6 of the ALU or CY is "1" as a result of an arithmetic operation. The flag is also set to "1" if the resultant product of executing a multiplication instruction (MUL AB) is greater than 0FFH, but is reset to "0" if the product is less than or equal to 0FFH.
PSW.3	RS0	RAM register bank switch
PSW.4	RS1	

RS1	RS0	BANK	RAM ADDRESS
0	0	0	00H – 07H
0	1	1	08H – 0FH
1	0	2	10H – 17H
1	1	3	18H – 1FH

PSW.5	F0	User flag which may be set to "0" or "1" as desired by the user.
PSW.6	AC	Auxiliary carry flag. This flag is set to "1" if a carry C_3 is generated from bit 3 of the ALU as a result of executing an arithmetic operation instruction. In all other cases, the flag is reset to "0".
PSW.7	CY	Main carry flag. This flag is set to "1" if a carry C_7 is generated from bit 7 of the ALU as result of executing an arithmetic operation instruction. If a carry C_7 is not generated, the flag is reset to "0".

I/O control register (IOCON)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
IOCON	0F8H	WDT	T32	SERR	IZC	P3HZ	P2HZ	P1HZ	ALF

BIT LOCATION	FLAG	FUNCTION
IOCON.0	ALF	If CPU power down mode (PD, HPD) is activated with this bit set to "1", the outputs from ports 0, 1, 2, and 3 are switched to floating status. When this bit is "0", ports 0, 1, 2, and 3 are in output mode.
IOCON.1	P1HZ	Port 1 becomes a high impedance input port when this bit is "1".
IOCON.2	P2HZ	Port 2 becomes a high impedance input port when this bit is "1".
IOCON.3	P3HZ	Port 3 becomes a high impedance input port when this bit is "1".
IOCON.4	IZC	The 10 kohm pull-up resistance for ports 1, 2, and 3 is switched off when this bit is "1", leaving only the 100 kohm pull-up resistance.
IOCON.5	SERR	Serial port reception error flag. This flag is set to "1" if an overrun or framing error is generated when data is received at a serial port. The flag is reset by software.
IOCON.6	T32	Timer/counters 0 and 1 are connected serially to form a 32-bit timer/counter when this bit is set to "1". TF1 of TCON is set if a carry is generated in the 32-bit timer/counter.
IOCON.7	WDT	Watchdog timer mode is set when this bit is set to "1". And if TF1 is set to "1" after watchdog timer mode has been set, the CPU is reset and the program is executed from address 0.

Timer 2 control register (T2CON)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
T2CON	0C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

BIT LOCATION	FLAG	FUNCTION
T2CON.0	CP/$\overline{RL2}$	Capture mode is set when TCLK + RCLK = "0" and CP/$\overline{RL2}$ = "1". 16-bit auto reload mode is set when TCLK + RCLK = "0" and CP/$\overline{RL2}$ = "0". CP/$\overline{RL2}$ is ignored when TCLK + RCLK = "1".
T2CON.1	C/$\overline{T2}$	Timer/counter 2 count clock designation control bit. The internal clocks (XTAL1·2 ÷ 12, XTAL1·2 ÷ 2) are used when this bit is "0", and the external clock applied to the T2 pin is passed to timer/counter 2 when the bit is "1".
T2CON.2	TR2	Timer/counter 2 counting start and stop control bit. Timer/counter 2 commences counting when this bit is "1" and stops counting when "0".
T2CON.3	EXEN2	T2EX timer/counter 2 external control signal control bit. Input of the T2EX signal is disabled when this bit is "0", and enabled when "1".
T2CON.4	TCLK	Serial port transmit circuit drive clock control bit. Timer/counter 2 is switched to baud rate generator mode when this bit is "1", and the timer/counter 2 carry signal becomes the serial port transmit clock. Note, however, that the serial ports can only use the timer/counter 2 carry signal in serial port modes 1 and 3.
T2CON.5	RCLK	Serial port receive circuit drive clock control bit. Timer/counter 2 is switched to baud rate generator mode when this bit is "1", and the timer/counter 2 carry signal becomes the serial port receive clock. Note, however, that the serial ports can only use the timer/counter 2 carry signal in serial port modes 1 and 3.
T2CON.6	EXF2	Timer/counter 2 external flag. This bit is set to "1" when the T2EX timer/counter 2 external control signal level is changed from "1" to "0" while EXEN2 = "1". This flag serves as the timer interrupt 2 request signal. If an interrupt is generated, EXF2 must be reset to "0" by software.
T2CON.7	TF2	Timer/counter 2 carry flag. This bit is set to "1" by a carry signal when timer/counter 2 is in 16-bit auto reload mode or in capture mode. This flag serves as the timer interrupt 2 request signal. If an interrupt is generated, TF2 must be reset to "0" by software.

LIST OF INSTRUCTIONS

LIST OF INSTRUCTION SYMBOLS

A	: Accumulator
AB	: Register pair
AC	: Auxiliary carry flag
B	: Arithmetic operation register
C	: Carry flag
DPTR	: Data pointer
PC	: Program counter
Rr	: Register indicator (r = 0 ~ 7)
SP	: Stack pointer
AND	: Logical product
OR	: Logical sum
XOR	: Exclusive OR
+	: Addition
−	: Subtraction
X	: Multiplication
/	: Division
(X)	: Denotes the contents of X
((X))	: Denotes the contents of address determined by the contents of X
#	: Denotes the immediate data
@	: Denotes the indirect address
=	: Equality
≠	: Non equality
←	: Substitution
→	: Substitution
¯	: Negation
<	: Smaller than
>	: Larger than
bit address	: RAM and the special function register bit specifier address ($b_0 \sim b_7$)
code address	: Absolute address ($A_0 \sim A_{15}$)
data	: Immediate data ($I_0 \sim I_7$)
relative offset	: Relative jump address offset value ($R_0 \sim R_7$)
direct address	: RAM and the special function register byte specifier address ($a_0 \sim a_7$)

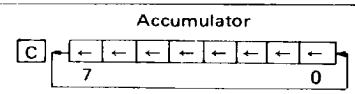
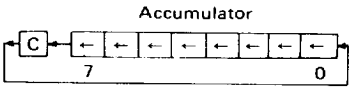
MSM80C154/MSM83C154 INSTRUCTION TABLE

L / H	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111
0 0000	NOP	AJMP address 11 (Page 0)	LJMP address 16	RR A	INC A	INC direct	INC @R0	INC @R1
1 0001	JBC bit, rel	ACALL address 11 (Page 0)	LCALL address 16	RRC A	DEC A	DEC direct	DEC @R0	DEC @R1
2 0010	JB bit, rel	AJMP address 11 (Page 1)	RET	RL A	ADD A, #data	ADD A, direct	ADD A, @R0	ADD A, @R1
3 0011	JNB bit, rel	ACALL address 11 (Page 1)	RETI	RLC A	ADDC A, #data	ADDC A, direct	ADDC A, @R0	ADDC A, @R1
4 0100	JC bit, rel	AJMP address 11 (Page 2)	ORL direct, A	ORL direct, #data	ORL A, #data	ORL A, direct	ORL A, @R0	ORL A, @R1
5 0101	JNC rel	ACALL address 11 (Page 2)	ANL direct, A	ANL direct, #data	ANL A, #data	ANL A, direct	ANL A, @R0	ANL A, @R1
6 0110	JZ rel	AJMP address 11 (Page 3)	XRL direct, A	XRL direct, #data	XRL A, #data	XRL A, direct	XRL A, @R0	XRL A, @R1
7 0111	JNZ rel	ACALL address 11 (Page 3)	ORL C, bit	JMP @A+DPTR	MOV A, #data	MOV direct, #data	MOV @R0, #data	MOV @R1, #data
8 1000	SJMP rel	AJMP address 11 (Page 4)	ANL C, bit	MOVC A, @A+PC	DIV AB	MOV direct 1, direct 2	MOV direct, @R0	MOV direct, @R1
9 1001	MOV DPTR #data 16	ACALL address 11 (Page 4)	MOV bit, C	MOVC A, @A+DPTR	SUBB A, #data	SUBB A, direct	SUBB A, @R0	SUBB A, @R1
A 1010	ORAL C, bit	AJMP address 11 (Page 5)	MOV C, bit	INC DPTR	MUL AB		MOV @R0, direct	MOV @R1, direct
B 1011	ANL C, bit	ACALL address 11 (Page 5)	CPL bit	CPL C	CJNE A, #data, rel	CJNE A, direct, rel	CJNE @R0, #data, rel	CJNE @R1, #data, rel
C 1100	PUSH direct	AJMP address 11 (Page 6)	CLR bit	CLR C	SWAP A	XCH A, direct	XCH A, @R0	XCH A, @R1
D 1101	POP direct	ACALL address 11 (Page 6)	SETB bit	SETB C	DA A	DJNZ direct, rel	XCHD A, @R0	XCH A, @R1
E 1110	MOVX A, @DPTR	AJMP address 11 (Page 7)	MOVX A, @R0	MOVX A, @R1	CLR A	MOV A, direct	MOV A, @R0	MOV A, @R1
F 1111	MOVX @DPTR, A	ACALL address 11 (Page 7)	MOVX @R0, A	MOVX @R1, A	CPL A	MOV direct, A	MOV @R0, A	MOV @R1, A

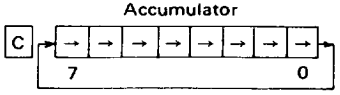
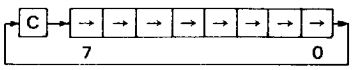
2 BYTE		3 BYTE
	MNEMONIC	
2 CYCLE		4 CYCLE

L / H	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111
0 0000	INC R0	INC R1	INC R2	INC R3	INC R4	INC R5	INC R6	INC R7
1 0001	DEC R0	DEC R1	DEC R2	DEC R3	DEC R4	DEC R5	DEC R6	DEC R7
2 0010	ADD A, R0	ADD A, R1	ADD A, R2	ADD A, R3	ADD A, R4	ADD A, R5	ADD A, R6	ADD A, R7
3 0011	ADDC A, R0	ADDC A, R1	ADDC A, R2	ADDC A, R3	ADDC A, R4	ADDC A, R5	ADDC A, R6	ADDC A, R7
4 0100	ORL A, R0	ORL A, R1	ORL A, R2	ORL A, R3	ORL A, R4	ORL A, R5	ORL A, R6	ORL A, R7
5 0101	ANL A, R0	ANL A, R1	ANL A, R2	ANL A, R3	ANL A, R4	ANL A, R5	ANL A, R6	ANL A, R7
6 0110	XRL A, R0	XRL A, R1	XRL A, R2	XRL A, R3	XRL A, R4	XRL A, R5	XRL A, R6	XRL A, R7
7 0111	MOV R0, #data	MOV R1, #data	MOV R2, #data	MOV R3, #data	MOV R4, #data	MOV R5, #data	MOV R6, #data	MOV R7, #data
8 1000	MOV direct, R0	MOV direct, R1	MOV direct, R2	MOV direct, R3	MOV direct, R4	MOV direct, R5	MOV direct, R6	MOV direct, R7
9 1001	SUBB A, R0	SUBB A, R1	SUBB A, R2	SUBB A, R3	SUBB A, R4	SUBB A, R5	SUBB A, R6	SUBB A, R7
A 1010	MOV R0, direct	MOV R1, direct	MOV R2, direct	MOV R3, direct	MOV R4, direct	MOV R5, direct	MOV R6, direct	MOV R7, direct
B 1011	CJNE R0, #data, rel	CJNE R1, #data, rel	CJNE R2, #data, rel	CJNE R3, #data, rel	CJNE R4, #data, rel	CJNE R5, #data, rel	CJNE R6, #data, rel	CJNE R7, #data, rel
C 1100	XCH A, R0	XCH A, R1	XCH A, R2	XCH A, R3	XCH A, R4	XCH A, R5	XCH A, R6	XCH A, R7
D 1101	DJNZ R0 rel	DJNZ R1 rel	DJNZ R2, rel	DJNZ R3, rel	DJNZ R4, rel	DJNE R5, rel	DJNE R6, rel	DJNE R7, rel
E 1110	MOV A, R0	MOV A, R1	MOV A, R2	MOV A, R3	MOV A, R4	MOV A, R5	MOV A, R6	MOV A, R7
F 1111	MOV R0, A	MOV R1, A	MOV R2, A	MOV R3, A	MOV R4, A	MOV R5, A	MOV R6, A	MOV R7, A

INSTRUCTION SET DETAILS

Type	Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Bytes	Cycles	Description
Arithmetic operation instructions	ADD A, Rr	0 0 1 0 1 r_2 r_1 r_0	1	1	(AC), (0V), (C), (A) ← (A)+(Rr)
	ADD A, direct	0 0 1 0 0 1 0 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(AC), (0V), (C), (A) ← (A)+(direct address)
	ADD A, @Rr	0 0 1 0 0 1 1 r_0	1	1	(AC), (0V), (C), (A) ← (A)+((Rr))
	ADD A, #data	0 0 1 0 0 1 0 0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	2	1	(AC), (0V), (C), (A) ← (A)+#data
	ADDC A, Rr	0 0 1 1 1 r_2 r_1 r_0	1	1	(AC), (0V), (C), (A) ← (A)+(C)+(Rr)
	ADDC A, direct	0 0 1 1 0 1 0 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(AC), (0V), (C), (A) ← (A)+(C)+(direct address)
	ADDC A, @Rr	0 0 1 1 0 1 1 r_0	1	1	(AC), (0V), (C), (A) ← (A)+(C)+((Rr))
	ADDC A, #data	0 0 1 1 0 1 0 0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	2	1	(AC), (0V), (C), (A) ← (A)+(C)+#data
	SUBB A, Rr	1 0 0 1 1 r_2 r_1 r_0	1	1	(AC), (0V), (C), (A) ← (A)−((C))+((Rr))
	SUBB A, direct	1 0 0 1 0 1 0 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(AC), (0V), (C), (A) ← (A)−((C)+(direct address))
	SUBB A, @Rr	1 0 0 1 0 1 1 r_0	1	1	(AC), (0V), (C), (A) ← (A)−((C)+((Rr))
	SUBB A, #data	1 0 0 1 0 1 0 0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	2	1	(AC), (0V), (C), (A) ← (A)−((C)+#data)
	MUL AB	1 0 1 0 0 1 0 0	1	4	(AB) ← (A) x (B)
	DIV AB	1 0 0 0 0 1 0 0	1	4	(A) quotient, (B) remainder ← (A)/(B)
	DA A	1 1 0 1 0 1 0 0	1	1	When the contents of accumulator bits 0 thru 3 are greater than 9, or when auxiliary carry (AC) is 1, 6 is added to bits 0 thru 3. Bits 4 thru 7 are then examined, and when bits 4 thru 7 following compensation of lower bits 0 thru 3 is greater than 9, or when carry (C) is 1, 6 is added to bits 4 thru 7. As a result, the carry flag can be set, but cannot be cleared.
Accumulation operation instructions	CLR A	1 1 1 0 0 1 0 0	1	1	(A) ← 0
	CPL A	1 1 1 1 0 1 0 0	1	1	(A) ← $\overline{(A)}$
	RL A	0 0 1 0 0 0 1 1	1	1	
	RLC A	0 0 1 1 0 0 1 1	1	1	

INSTRUCTION SET DETAILS (CONT.)

Type	Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Bytes	Cycles	Description
Accumulator operation instructions	RR A	0 0 0 0 0 0 1 1	1	1	
	RRC A	0 0 0 1 0 0 1 1	1	1	
	SWAP A	1 1 0 0 0 1 0 0	1	1	$(A_4 \sim _7) \rightleftharpoons (A_0 \sim _3)$
Increment/decrement	INC A	0 0 0 0 0 1 0 0	1	1	(A) ← (A)+1
	INC Rr	0 0 0 0 1 r_2 r_1 r_0	1	1	(Rr) ← (Rr)+1
	INC direct	0 0 0 0 0 1 0 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(direct address) ← (direct address)+1
	INC @Rr	0 0 0 0 0 1 1 r_0	1	1	((Rr)) ← ((Rr))+1
	INC DPTR	1 0 1 0 0 0 1 1	1	2	(DPTR) ← (DPTR)+1
	DEC A	0 0 0 1 0 1 0 0	1	1	(A) ← (A)−1
	DEC Rr	0 0 0 1 1 r_2 r_1 r_0	1	1	(Rr) ← (Rr)−1
	DEC direct	0 0 0 1 0 1 0 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(direct address) ← (direct address)−1
	DEC @Rr	0 0 0 1 0 1 1 r_0	1	1	((Rr)) ← ((Rr))−1
Logical operation instructions	ANL A, Rr	0 1 0 1 1 r_2 r_1 r_0	1	1	(A) ← (A) AND (Rr)
	ANL A, direct	0 1 0 1 0 1 0 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(A) ← (A) AND (direct address)
	ANL A, @Rr	0 1 0 1 0 1 1 r_0	1	1	(A) ← (A) AND ((Rr))
	ANL A, #data	0 1 0 1 0 1 0 0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	2	1	(A) ← (A) AND #data
	ANL direct, A	0 1 0 1 0 0 1 0 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(direct address) ← (direct address) AND (A)
	ANL direct, #data	0 1 0 1 0 0 1 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	3	2	(direct address) ← (direct address) AND #data
	ORL A, Rr	0 1 0 0 1 r_2 r_1 r_0	1	1	(A) ← (A) OR (Rr)
	ORL A, direct	0 1 0 0 0 1 0 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(A) ← (A) OR (direct address)
	ORL A, @Rr	0 1 0 0 0 1 1 r_0	1	1	(A) ← (A) OR ((Rr))
	ORL A, #data	0 1 0 0 0 1 0 0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	2	1	(A) ← (A) OR #data

INSTRUCTION SET DETAILS (CONT.)

Type	Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Bytes	Cycles	Description
Logical operation instructions	ORL direct, A	0 1 0 0 0 0 1 0 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(direct address) ← (direct address) OR (A)
	ORL direct, #data	0 1 0 0 0 0 1 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	3	2	(direct address) ← (direct address) OR #data
	XRL A, Rr	0 1 1 0 1 r_2 r_1 r_0	1	1	(A) ← (A) XOR (Rr)
	XRL A, direct	0 1 1 0 0 1 0 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(A) ← (A) XOR (direct address)
	XRL A, @Rr	0 1 1 0 0 1 1 r_0	1	1	(A) ← (A) XOR ((Rr))
	XRL A, #data	0 1 1 0 0 1 0 0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	2	1	(A) ← (A) XOR #data
	XRL direct, A	0 1 1 0 0 0 1 0 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(direct address) ← (direct address) XOR (A)
	XRL direct, #data	0 1 1 0 0 0 1 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	3	2	(direct address) ← (direct address) XOR #data
Immediate data setting instructions	MOV A, #data	0 1 1 1 0 1 0 0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	2	1	(A) ← #data
	MOV Rr, #data	0 1 1 1 1 r_2 r_1 r_0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	2	1	(Rr) ← #data
	MOV direct, #data	0 1 1 1 0 1 0 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	3	2	(direct address) ← #data
	MOV @Rr, #data	0 1 1 1 0 1 1 r_0 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	2	1	(Rr)) ← #data
	MOV DPTR, #data 16	1 0 0 1 0 0 0 0 I_{15} I_{14} I_{13} I_{12} I_{11} I_{10} I_9 I_8 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	3	2	(DPTR) ← #data 16
Carry flag operation instructions	CLR C	1 1 0 0 0 0 1 1	1	1	(C) ← 0
	SETB C	1 1 0 1 0 0 1 1	1	1	(C) ← 1
	CPL C	1 0 1 1 0 0 1 1	1	1	(C) ← $\overline{(C)}$
	ANL C, bit	1 0 0 0 0 0 1 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0	2	2	(C) ← (C) AND (bit address)
	ANL C,/bit	1 0 1 1 0 0 0 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0	2	2	(C) ← (C) AND $\overline{\text{(bit address)}}$
	ORL C, bit	0 1 1 1 0 0 1 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0	2	2	(C) ← (C) OR (bit address)
	ORL C,/bit	1 0 1 0 0 0 0 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0	2	2	(C) ← (C) OR $\overline{\text{(bit address)}}$
	MOV C, bit	1 0 1 0 0 0 1 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0	2	1	(C) ← (bit address)

INSTRUCTION SET DETAILS (CONT.)

Type	Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Bytes	Cycles	Description
	MOV bit, C	1 0 0 1 0 0 1 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0	2	2	(bit address) ← (C)
Bit operation instructions	SETB bit	1 1 0 1 0 0 1 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0	2	1	(bit address) ← 1
	CLR bit	1 1 0 0 0 0 1 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0	2	1	(bit address) ← 0
	CPL bit	1 0 1 1 0 0 1 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0	2	1	(bit address) ← $\overline{\text{(bit address)}}$
Data transfer instructions	MOV A, Rr	1 1 1 0 1 r_2 r_1 r_0	1	1	(A) ← (Rr)
	MOV A, direct	1 1 1 0 0 1 0 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(A) ← (direct address)
	MOV A, @Rr	1 1 1 0 0 1 1 r_0	1	1	(A) ← ((Rr))
	MOV Rr, A	1 1 1 1 1 r_2 r_1 r_0	1	1	(Rr) ← (A)
	MOV Rr, direct	1 0 1 0 1 r_2 r_1 r_0 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	2	(Rr) ← (direct address)
	MOV direct, A	1 1 1 1 0 1 0 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(direct address) ← (A)
	MOV direct, Rr	1 0 0 0 1 r_2 r_1 r_0 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	2	(direct address) ← (Rr)
	MOV direct, @Rr	1 0 0 0 0 1 1 r_0 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	2	(direct address) ← ((Rr))
	MOV @Rr, A	1 1 1 1 0 1 1 r_0	1	1	((Rr)) ← (A)
	MOV @Rr, direct	1 0 1 0 0 1 1 r_0 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	2	((Rr)) ← (direct address))
Constant code instructions	MOVC A, @A+DPTR	1 0 0 1 0 0 1 1	1	2	(A) ← ((A) + (DPTR))
	MOVC A,@A+PC	1 0 0 0 0 0 1 1	1	2	(PC) ← (PC) + 1 (A) ← ((A) + (PC))
Data exchange instructions	XCH A, Rr	1 1 0 0 1 r_2 r_1 r_0	1	1	(A) ⇌ (Rr)
	XCH A, direct	1 1 0 0 0 1 0 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	1	(A) ⇌ (direct address)
	XCH A, @Rr	1 1 0 0 0 1 1 r_0	1	1	(A) ⇌ ((Rr))
	XCHD A, @Rr	1 1 0 1 0 1 1 r_0	1	1	($A_0 \sim _3$) ⇌ (($Rr_0 \sim _3$))

INSTRUCTION SET DETAILS (CONT.)

Type	Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Bytes	Cycles	Description
Subroutine instructions	PUSH direct	1 1 0 0 0 0 0 0 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	2	(SP) ← (SP)+1 ((SP)) ← (direct address)
	POP direct	1 1 0 1 0 0 0 0 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	2	2	(direct address) ← ((SP)) (SP) ← (SP)−1
	ACALL addr 11	A_{10} A_9 A_8 1 0 0 0 1 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0	2	2	(PC) ← (PC)+2 (SP) ← (SP)+1 ((SP)) ← ($PC_0 \sim_7$) (SP) ← (SP)+1 ((SP)) ← ($PC_8 \sim_{15}$) ($PC_0 \sim_{10}$) ← $A_0 \sim_{10}$
	LCALL addr 16	0 0 0 1 0 0 1 0 A_{15} A_{14} A_{13} A_{12} A_{11} A_{10} A_9 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0	3	2	(PC) ← (PC)+3 (SP) ← (SP)+1 ((SP)) ← ($PC_0 \sim_7$) (SP) ← (SP)+1 ((SP)) ← ($PC_8 \sim_{15}$) ($PC_0 \sim_{15}$) ← $A_0 \sim_{15}$
	RET	0 0 1 0 0 0 1 0	1	2	($PC_8 \sim_{15}$) ← ((SP)) (SP) ← (SP)−1 ($PC_0 \sim_7$) ← ((SP)) (SP) ← (SP)−1
	RETI	0 0 1 1 0 0 1 0	1	2	($PC_8 \sim_{15}$) ← ((SP)) (SP) ← (SP)−1 ($PC_0 \sim_7$) ← ((SP)) (SP) ← (SP)−1
Jump instructions	AJMP addr 11	A_{10} A_9 A_8 0 0 0 0 1 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0	2	2	(PC) ← (PC)+2 ($PC_0 \sim_{10}$) ← $A_0 \sim_{10}$
	LJMP addr 16	0 0 0 0 0 0 1 0 A_{15} A_{14} A_{13} A_{12} A_{11} A_{10} A_9 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0	3	2	($PC_0 \sim_{15}$) ← $A_0 \sim_{15}$
	SJMP rel	1 0 0 0 0 0 0 0 R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	2	2	(PC) ← (PC)+2 (PC) ← (PC)+relative offset
	JMP @A+DPTR	0 1 1 1 0 0 1 1	1	2	(PC) ← (A)+(DPTR)

Branch instructions	CJNE A, direct, rel	1 0 1 1 0 1 0 1
		a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0
		R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0
			3	2	(PC) ← (PC)+3
					IF (A) ≠ (direct address)
					THEN
					(PC) ← (PC)+relative offset
					IF (A) < (direct address)
					THEN
					(C) ← 1
					ELSE
					(C) ← 0

	CJNE A, #data, rel	1 0 1 1 0 1 0 0
		I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0
		R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0
			3	2	(PC) ← (PC)+3
					IF (A) ≠ #data
					THEN
					(PC) ← (PC)+relative offset
					IF (A) < #data
					THEN
					(C) ← 1
					ELSE
					(C) ← 0

INSTRUCTION SET DETAILS (CONT.)

Type	Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Bytes	Cycle	Description

Branch instructions	CJNE Rr, #data, rel	1 0 1 1 1 r_2 r_1 r_0
		I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0
		R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0
			3	2	(PC) ← (PC)+3
					IF ((Rr)) ≠ #data
					THEN
					(PC) ← (PC)+relative offset
					IF ((Rr)) < #data
					THEN
					(C) ← 1
					ELSE
					(C) ← 0

	CJNE @Rr, #data, rel	1 0 1 1 0 1 1 r_0
		I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0
		R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0
			3	2	(PC) ← (PC)+3
					IF ((Rr)) ≠ #data
					THEN
					(PC) ← (PC)+relative offset
					IF ((Rr)) < #data
					THEN
					(C) ← 1
					ELSE
					(C) ← 0

	DJNZ Rr, rel	1 1 0 1 1 r_2 r_1 r_0 R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	2	2	(PC) ← (PC)+2 (Rr) ← (Rr)−1 IF (Rr) ≠ 0 THEN (PC) ← (PC)+relative offset
	DJNZ direct, rel	1 1 0 1 0 1 0 1 a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0 R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	3	2	(PC) ← (PC)+3 (direct address) ← (direct address)−1 IF (direct address) ≠ 0 THEN (PC) ← (PC)+relative offset
	JZ rel	0 1 1 0 0 0 0 0 R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	2	2	(PC) ← (PC)+2 IF (A) = 0 THEN (PC) ← (PC)+relative offset
	JNZ rel	0 1 1 1 0 0 0 0 R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	2	2	(PC) ← (PC)+2 IF (A) ≠ 0 THEN (PC) ← (PC)+relative offset
	JC rel	0 1 0 0 0 0 0 0 R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	2	2	(PC) ← (PC)+2 IF (C) = 1 THEN (PC) ← (PC)+relative offset
	JNC rel	0 1 0 1 0 0 0 0 R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	2	2	(PC) ← (PC)+2 IF (C) = 0 THEN (PC) ← (PC)+relative offset
	JB bit, rel	0 0 1 0 0 0 0 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0 R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	3	2	(PC) ← (PC)+3 IF (bit address) = 1 THEN (PC) ← (PC)+relative offset
	JNB bit, rel	0 0 1 1 0 0 0 0 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0 R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	3	2	(PC) ← (PC)+3 IF (bit address) = 0 THEN (PC) ← (PC)+relative offset

INSTRUCTION SET DETAILS (CONT.)

Type	Mnemonic	Instruction Code								Bytes	Cycle	Description
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			
Branch instructions	JBC bit, rel	0 b_7 R_7	0 b_6 R_6	0 b_5 R_5	1 b_4 R_4	0 b_3 R_3	0 b_2 R_2	0 b_1 R_1	0 b_0 R_0	3	2	(PC) ← (PC)+3 IF (bit address) = 1 THEN (bit address) ← 0 (PC) ← (PC)+relative offset
External memory instructions	MOVX A, @Rr	1	1	1	0	0	0	1	r_0	1	2	(A) ← ((Rr)) EXTERNAL RAM
	MOVX A, @DPTR	1	1	1	0	0	0	0	0	1	2	(A) ← ((DPTR)) EXTERNAL RAM
	MOVX @Rr, A	1	1	1	1	0	0	1	r_0	1	2	(Rr) ← (A) EXTERNAL RAM
	MOVX @DPTR, A	1	1	1	1	0	0	0	0	1	2	((DPTP)) ← (A) EXTERNAL RAM
Other instructions	NOP	0	0	0	0	0	0	0	0	1	1	(PC) ← (PC)+1

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	Vcc	Ta = 25 °C	−0.5 ~ 7	V
Input voltage	V_I	Ta = 25 °C	−0.5 ~ Vcc + 0.5	V
Storage temperature	Tstg		−55 ~ + 150	°C

Operational Range

- MSM80C154/83C154 ...DC to 12 MHz, VCC = 5V±20%
- MSM80C154-1/83C154-1 ...DC to 16 MHz, VCC = 5V±5%

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	Vcc	*1 fosc = DC-16 MHz	2.5 ~ 6	V
Memory hold voltage	Vcc		2 ~ 6	V
Ambient temperature	Ta		−40 ~ +85 (0 ~ 12 MHz) −20 ~ +70 (12 ~ 16 MHz)	°C

*1: 2.5 V ≤ Vcc < 4 V DC characteristics will be specified elsewhere.

DC Characteristics

(V_{CC} = 5V±10%, Ta = −40 to +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Measuring circuit
Input Low Voltage	V_{IL}		−0.5		0.2 V_{CC}−0.1	V	1
Input High Voltage	V_{IH}	Except XTAL1 and RESET	0.2 V_{CC} +0.9		V_{CC} + 0.5	V	
Input High Voltage	V_{IHI}	XTAL1 and RESET	0.7 V_{CC}		V_{CC} + 0.5	V	
Output Low Voltage (PORT 1, 2, 3)	V_{OL}	I_{OL} = 1.6 mA			0.45	V	
Output Low Voltage (PORT 0, ALE, PSEN)	V_{OL1}	I_{OL} = 3.2 mA			0.45	V	
Output High Voltage (PORT 1, 2, 3)	V_{OH}	I_{OH} = −60 μA V_{CC} = 5 V ± 10%	2.4			V	
		I_{OH} = −30 μA	0.75 V_{CC}			V	
		I_{OH} = −10 μA	0.9 V_{CC}			V	
Output High Voltage (PORT 0, ALE, PSEN)	V_{OHI}	I_{OH} = −400 μA V_{CC} = 5 V ± 10%	2.4			V	
		I_{OH} = −150 μA	0.75 V_{CC}			V	
		I_{OH} = −40 μA	0.9 V_{CC}			V	
Logical 0 Input Current/ Logical 1 Output Current (PORT 1, 2, 3)	I_{IL}/I_{OH}	V_I=0.45V / V_O=0.45V	−10		−200	μA	2
Logical 1 to 0 Transition Current (PORT 1, 2, 3)	I_{TL}	V_I = 2.0 V			−500	μA	
Input Leakage Current (PORT 0 floating, EA)	I_{LI}	$V_{SS} < V_I < V_{CC}$			± 10	μA	3
RESET Pulldown Resistor	R_{RST}		20	40	125	KΩ	2
Pin Capacitance	C_{IO}	T_A = 25°C, f = 1 MHz 5 V (except XTAL1)			10	pF	
Power Down Current	I_{PD}	V_{CC} = 2 ~ 6 V		1	50	μA	4

Maximum Power Supply Current
Normal Operation I_{CC} (mA)

V_{CC}	4 V	5 V	6 V
Freq			
0.5 MHz	1.6	2.2	3
3.5 MHz	4.3	5.7	7.5
8 MHz	8.3	11	14
12 MHz	12	16	20

Maximum Power Supply Current
Idle Mode I_{CC} (mA)

V_{CC}	4 V	5 V	6 V
Freq			
0.5 MHz	0.6	0.9	1.2
3.5 MHz	1.1	1.6	2.2
8 MHz	1.8	2.7	3.7
12 MHz	2.5	3.7	5

*1: 2.5 V ≤ V_{CC} < 4 V DC characteristics will be specified elsewhere.

Maximum Power Supply Current
Normal Operation I_{CC} (mA)

V_{CC}	4.5 V	5 V	5.5 V
Freq.			
1.2 MHz	2.0	2.3	2.6
8 MHz	10	11	12.5
12 MHz	14	16	18

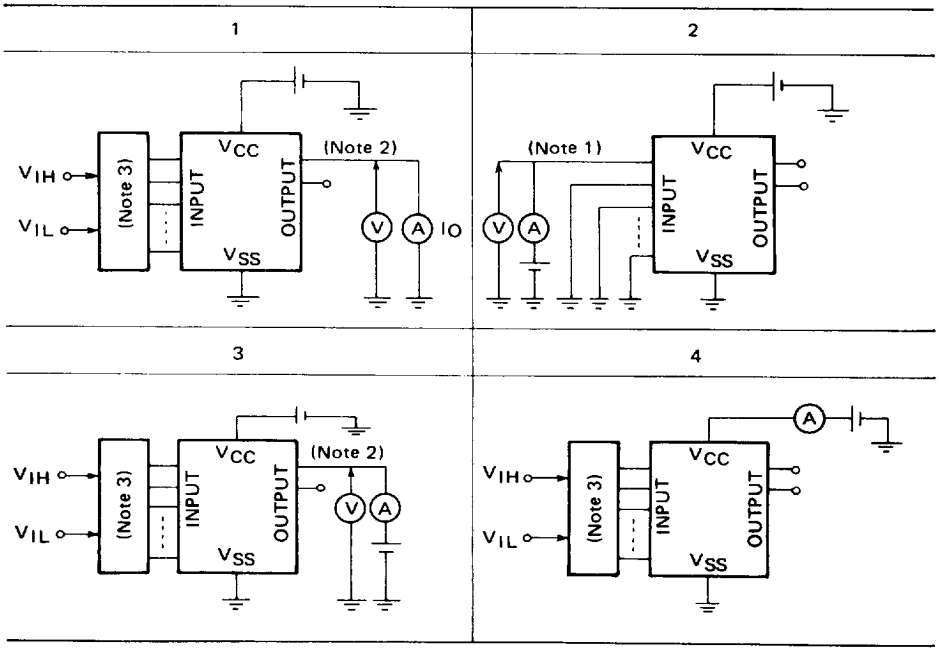
V_{CC}	4.75 V	5 V	5.25 V
Freq.			
16 MHz	18	20	23

Maximum Power Supply Current
Idle Mode I_{CC} (mA)

V_{CC}	4.5 V	5 V	5.5 V
Freq.			
1.2 MHz	1.4	1.5	1.6
8 MHz	2.3	2.7	3.2
12 MHz	3.0	3.7	5.0

V_{CC}	4.75 V	5 V	5.25 V
Freq.			
16 MHz	4.0	5.0	6.0

Measuring Circuits



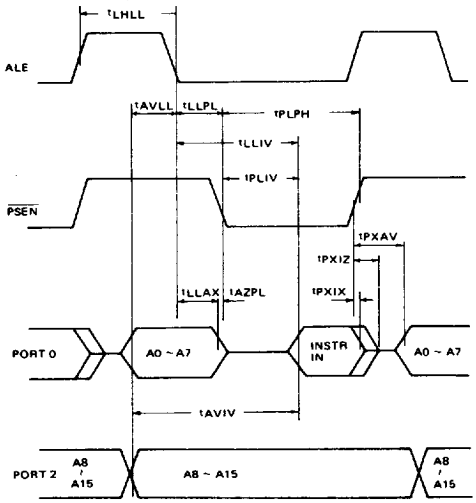
Note 1. Repeated for specified input pins.
2. Repeated for specified output pins.
3. Input logic for specified status.

External Program Memory Access AC Characteristics

(V_{CC} = 5 V ± 20%, V_{SS} = 0 V, XTAL1·2 = 12 MHz, Ta = −40 °C to 85 °C
V_{CC} = 5 V ± 5%, V_{SS} = 0 V, 12 MHz < XTAL1·2 < 16 MHz, Ta = − 20°C to 70°C
PORT 0, ALE, and $\overline{PSEN}$ connected with 100 pF load, other connected with 80 pF load)

Parameter	Symbol	Ratings				Unit
		16 MHz clock		Variable clock from DC to 16 MHz		
		Min.	Max.	Min.	Max.	
XTAL1·2 Oscillator Period	tCLCL	62.5		62.5		ns
ALE Pulse Width	tLHLL	85		2tCLCL-40		ns
Address Valid to ALE Low	tAVLL	18.5		1tCLCL-44		ns
Address Hold After ALE Low	tLLAX	27.5		1tCLCL-35		ns
ALE Low to Valid Instr In	tLLIV		150		4tCLCL-100	ns
ALE Low to $\overline{PSEN}$ Low	tLLPL	32.5		1tCLCL-30		ns
$\overline{PSEN}$ Pulse Width	tPLPH	152.5		3tCLCL-35		ns
$\overline{PSEN}$ Low to Valid Instr In	tPLIV		82.5		3tCLCL-105	ns
Input Instr Hold After $\overline{PSEN}$	tPXIX	0		0		ns
Input Instr Float After $\overline{PSEN}$	tPXIZ		42.5		1tCLCL-20	ns
$\overline{PSEN}$ to Address Valid	tPXAV	42.5		1tCLCL-20		ns
Address to Valid Instr In	tAVIV		207.5		5tCLCL-105	ns
Address Float to $\overline{PSEN}$ Low	tAZPL	0		0		ns

External program memory read cycle



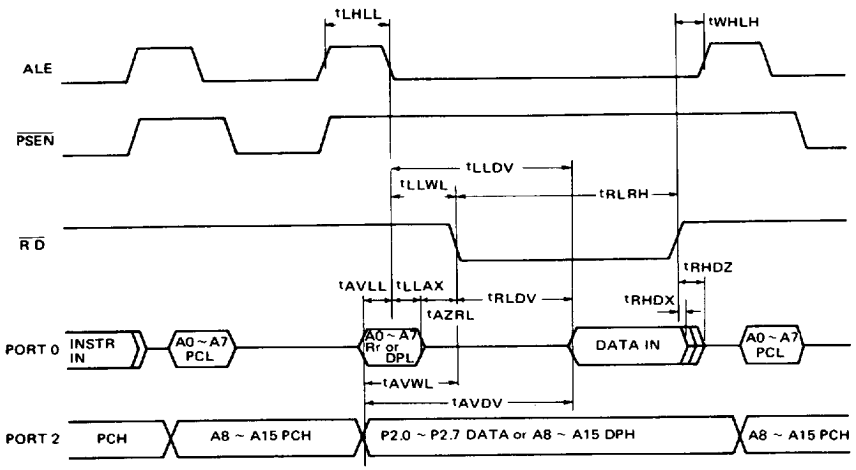
External Program Memory Access AC Characteristics

(V_{CC} = 5 V ± 20%, V_{SS} = 0 V, XTAL1·2 = 12 MHz, Ta = −40 °C to 85 °C
V_{CC} = 5 V ± 5%, V_{SS} = 0 V, 12 MHz < XTAL1·2 ≤ 16 MHz, Ta = − 20°C to 70°C

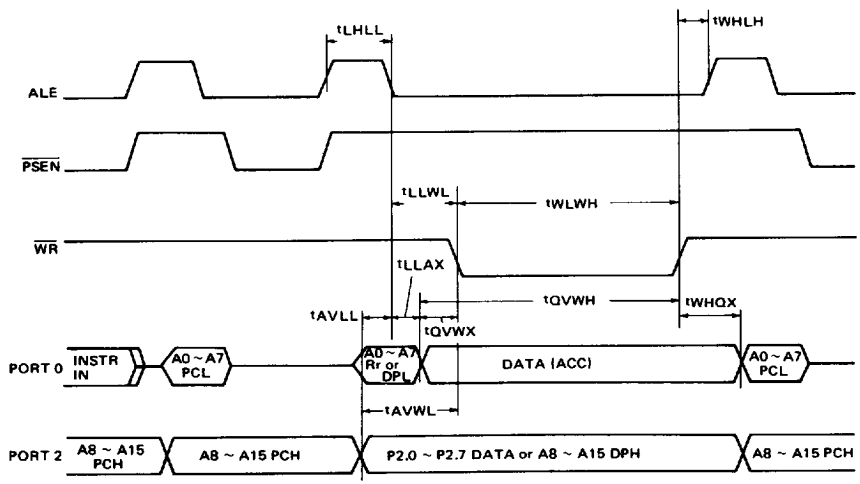
PORT 0, ALE, and $\overline{PSEN}$ connected with 100 pF load, other connected with 80 pF load)

Parameter	Symbol	Ratings				Unit
		16 MHz clock		Variable clock from DC to 16 MHz		
		Min.	Max.	Min.	Max.	
XTAL1·2 Oscillator Period	tCLCL	62.5		62.5		ns
ALE Pulse Width	tLHLL	85		2tCLCL-40		ns
Address Valid to ALE Low	tAVLL	18.5		1tCLCL-44		ns
Address Hold After ALE Low	tLLAX	27.5		1tCLCL-35		ns
$\overline{RD}$ Pulse Width	tRLRH	275		6tCLCL-100		
$\overline{WR}$ Pulse Width	tWLWH	275		6tCLCL-100		ns
$\overline{RD}$ Low to Valid Data In	tRLDV		207.5		5tCLCL-105	ns
Data Hold After $\overline{RD}$	tRHDX	0		0		ns
Data Float After $\overline{RD}$	tRHDZ		55		2tCLCL-70	ns
ALE Low to Valid Data In	tLLDV		400		8tCLCL-100	ns
Address to Valid Data In	tAVDV		457.5		9tCLCL-105	ns
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	tLLWL	147.5	227.5	3tCLCL-40	3tCLCL+40	ns
Address to $\overline{RD}$ or $\overline{WR}$ Low	tAVWL	180		4tCLCL-70		ns
Data Valid to $\overline{WR}$ Transition	tQVWX	22.5		1tCLCL-40		ns
Data Valid to $\overline{WR}$ High	tQVWH	332.5		7tCLCL-105		ns
Data Hold After $\overline{WR}$	tWHQX	75		2tCLCL-50		ns
Address Float to $\overline{RD}$ Low	tAZRL		0		0	ns
$\overline{RD}$ or $\overline{WR}$ High to ALE High	tWHLH	32.5	102.5	1tCLCL-30	1tCLCL+40	ns

External data memory read cycle



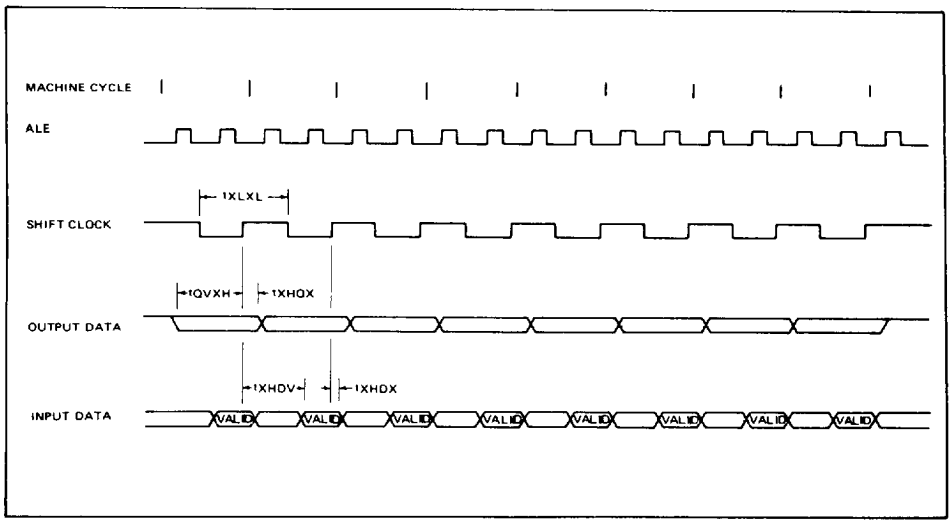
External data memory write cycle



Serial Port (I/O Extension Mode) AC Characteristics

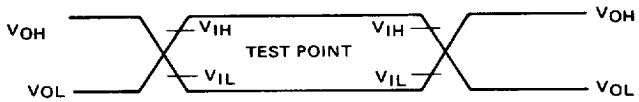
V_{CC} = 5 V ±20%, V_{SS} = 0 V, XTAL1·2 = 12 MHz, Ta = –40 °C to 85 °C
V_{CC} = 5 V ± 5%, V_{SS} = 0 V, 12 MHz < XTAL1·2 ≤ 16 MHz, Ta = – 20°C to 70°C

Parameter	Symbol	Min.	Max.	Unit
Serial Port Clock Cycle Time	tXLXL	12tCLCL		ns
Output Data Setup to Clock Rising Edge	tQVXH	10tCLCL-133		ns
Output Data Hold After Clock Rising Edge	tXHQX	2tCLCL-75		ns
Input Data Hold After Clock Rising Edge	tXHDX	0		ns
Clock Rising Edge to Input Data Valid	tXHDV		10tCLCL-133	ns



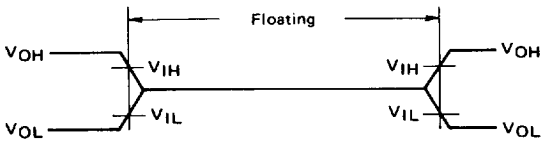
AC Characteristics Measuring Conditions

1. Input/output signal



* The input signals in AC test mode are either V_{OH} (logic "1") or V_{OL} (logic "0") input signals where logic "1" corresponds to a CPU output signal waveform measuring point in excess of V_{IH}, and logic "0" to a point below V_{IL}.

2. Floating



* The port 0 floating interval is measured from the time the port 0 pin voltage drops below V_{IH} after sinking to GND at 2.4 mA when switching to floating status from a "1" output, and from the time the port 0 pin voltage exceeds V_{IL} after connecting to a 400 μA source when switching to floating status from a "0" output.

XTAL1 External Clock Input Waveform Conditions

Parameter	Symbol	Min.	Max.	Units
Oscillator Freq.	1/tCLCL	DC	16	MHz
High Time	tCHCX	20		ns
Low Time	tCLCX	20		ns
Rise Time	tCLCH		20	ns
Fall Time	tCHCL		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM