FAIRCHILD
SEMICONDUCTOR™

Preliminary
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FM3570
CPU CONFIGURATION CONTROLLER
Register/Multiplexer for Microprocessor VID

General Description

The Fairchild FM3570 replaces the CPU motherboard's configuration switches with an electronic implementation consisting of a 4/5-bit multiplexed, 1-bit latched port, standard 2-wire bus interface, and non-volatile latches.

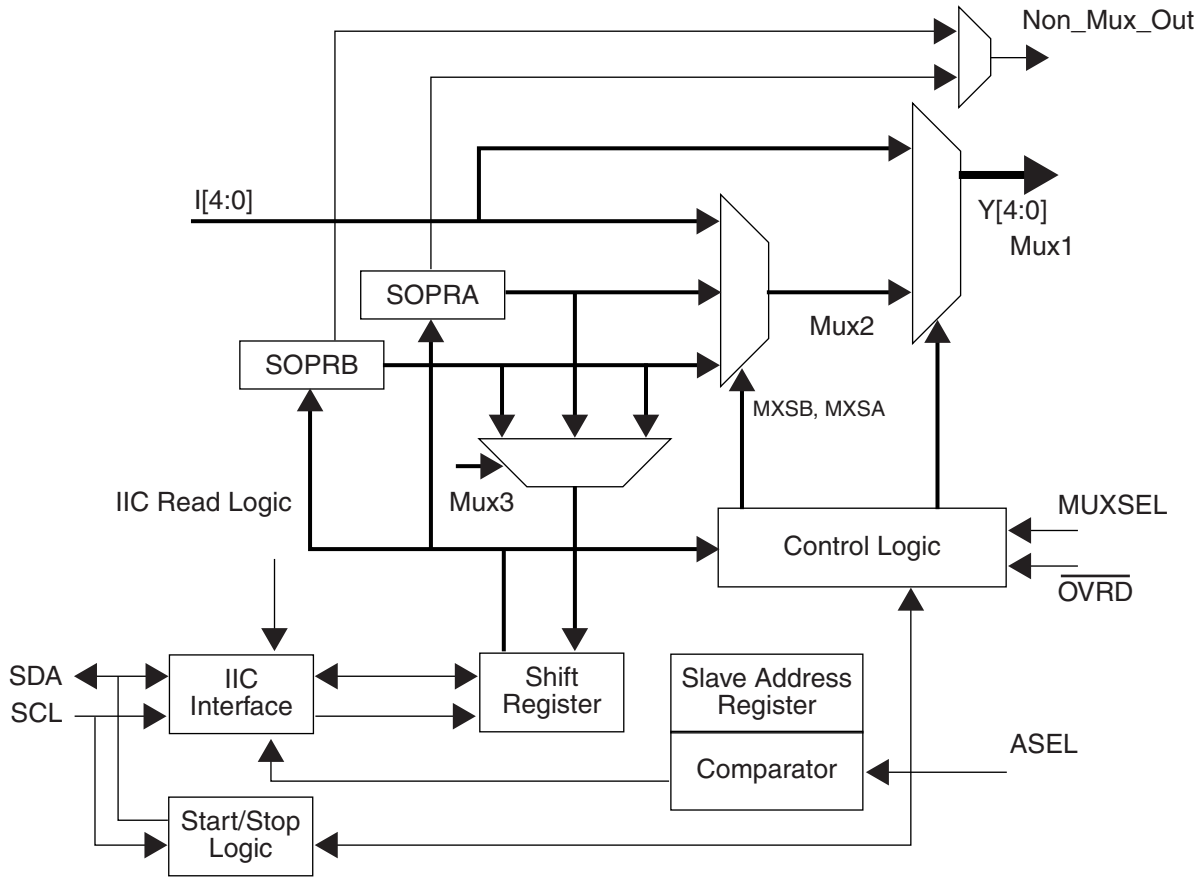
The FM3570 multiplexes the I-port input signals with two internal non-volatile registers that can be loaded through the serial port. The multiplexer is selected via the serial port and defaults to the I-port upon power-up. Pull-up resistors are provided on the input port to accommodate connections to open-drain outputs and to eliminate the need for external resistors. The device has open-drain outputs for easy interface to devices with different V_{DD} levels.

The serial port is an IIC compatible slave-only interface and supports both 100kbit and 400kbit modes of operation. The port is used to read the I-Port, write data to the internal non-volatile registers and select whether the I-port or one of the internal non-volatile registers is output to the Y-port. The FM3570 is fabricated with advanced CMOS technology to achieve high density and low power operation.

Features

- Extended Operating Voltage Range 3.0V-5.5V
- IIC Compatible Slave Interface.
- ESD performance: Human body model > 2000V
- Choice of 2.5V Outputs or Open-Drain Outputs

Block Diagram



Ordering Code

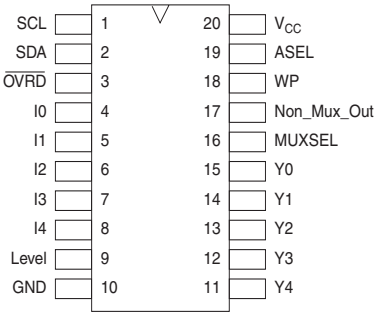
FM 3570 XXXX X

Blank	Tube
X	Tape & Reel
M20	20-Pin SO Package Option
MT20	20-Pin TSSOP Package Option

Order Number	Package Number	Package Description
FM3570MT20	MTC20	20-Pin TSSOP
FM3570MT20X	MTC20	20-Pin TSSOP T & R
FM3570M20	M20B	20 Pin SO
FM3570M20X	M20B	20 Pin SO T & R
For all other combinations, check with Fairchild Marketing/Sales		

Pin Connection Diagram

20-Pin Packages
FM3570



Pin Description

Pin Name	Description
I [0:4]	Data Inputs w/Pullups (10K-40K)
Y [0:4]	Open-Drain Data Outputs
SCL	Serial Port Clock Input (120K pullup)
$\overline{\text{OVRD}}$	Override Input. Sets all outputs to 0
WP	Write Protect Input
Non_mux_out	Non-Multiplexed Output
MUXSEL	Multiplexer Select Input
EPV	I Port Pull-up Resistor Voltage
ASEL	Address Select Input
SDA	Serial Port Data I/O (120K pull-up)

Functional Description

The FM3570 block diagram is shown in Figure 1. The device has two primary functional modes of operationi and an additional mode for programming the device.

Operational Modes

During standard operation, the device will either pass an address to the Y-Port from the I-Port or from an internally programmed value.

The I-port values are generated from the motherboard of the system and may be hardwired or driven by another device. Pull-up resistors are provided on the device to accommodate this device being driven by open-drain output drivers. The voltage level to which the I-port is pulled up to is determined by the voltage on the EPV pin. The device expects standard CMOS input signals. The the non-multiplexed output is always at CMOS levels. The $\overline{\text{OVRD}}$ (override) input, when set to 0, will cause all the outputs to be set to 0. The WP signal, if set to logic 1, will prevent data from being written to the non-volatile register.

The MUXSEL input, when set to logic 0, will select the data from the non-volatile register to drive on the Y0-4 outputs. if set to logic 1, the data from the inputs are selected instead. the non_mux_out latch is transparent when the MUXSEL signal is at logic 0, and will latch when the MUXSEL is in a logic 1 state.

Output Port: Y0-Y4

The output port is an open-drain output to allow for easy connection to devices running at different voltage levels. The port is always active and either passes the value on the I-Port or the value in the Serial output port (SOPR). Changing the Mux Path is accomplished by writing to b7 of the Serial Input Port Register. SOPR-b7 defaults to a value of zero at power up and the default path is from the I-port though to the output port. The multiplexer only updates when an IIC stop condition is observed.

Register Description

The FM3570 has 3 registers in total. These registers are made up of a combination of read-only, write-only and read/write bits. The two registers are listed below.

Serial Output Port Register A(SOPRA) Address: 00H - A read/write register that contains the new value to be written to output Port-Y and the multiplexer select bit.

Serial Output Port Register B(SOPRB) Address: 01H - A read/write register that contains the new value to be written to output Port-Y and the multiplexer select bit.

Parallel Input Port Register (PIPR) Address: 02H - A read-only register that is loaded with the 5-bit value of the I-Port.

Serial Output Port Register (SOPR)

(Address 000b and 001b)

MXSB	MXSA	Data Field					
0	0	I5	NMO	I3	I2	I1	I0
b7	b6	b5	b4	b3	b2	b1	b0

b7-b6 - Multiplexer Select Bits (MXSB, MXSA)

00 - Multiplexer passes the SOPR(A).

01 - Multiplexer passer the SOPR(B).

10 - Multiplexer defaults to passing the I-Port Value.

b5, b3-b0 - Data Field. New value to be output through the multiplexer.

NMO - Non-multiplexed output from internal non-volatile bit.

Parallel Input Port Register (PIPR)

(Address 002b)

Address Field			Data Field				
0	0	0	I4	I3	I2	I1	I0
b7	b6	b5	b4	b3	b2	B1	b0

b7-b5 - Address field. Value is always 000

b4-b0 - Data Field. Value is equal to the value on the I-Port.

The external Port Register captures the value on the I-Port. Data is latched into this register on the first clock after a start condition is seen. This insures that a valid value will always be in this register if it is read. This register is a-read only register with respect to the IIC port.

$\overline{OVRD}$	MUXSEL	MXSB	MXSA	Mux_ outputs	Non_mux_ ouput
0	0	X	X	all 0's	all 0's
0	1	X	X	Mux_ inputs	latched NMO (see Note 1)
1	0	1	0	Mux_ inputs	latched NMO (see Note 1)
1	0	0	0	From Non-volatile register (SOPRA)	From Non-volatile register (SOPRA)
1	0	1	1	Do not use this combination	
1	0	0	1	From Non-volatile register (SOPRB)	From Non-volatile register (SOPRB)
1	1	Note 2	Note 1	Mux_i nputs	From Non-volatile register (SOPRA or SOPRB)

Note 1: Latched NMO state will be the value present on the NMO output at the time of the MUXSEL input transitioning from logic 0 to logic 1 state.

Note 2: Output depends on previously selected state of MXSB and MXSA bits written to device.

Multiplexer Logic

The output multiplexer logic determines what value is actually output to the Y-port. The value that it output is dependent upon b7-b6 of the SOPRA and SOPRB registers, as well as the external MUXSEL and $\overline{OVRD}$ inputs. There is only one set of MXS bits in the SOPRA and SOPRB registers. Regardless of whether one writes to SPRA or SOPRB register for setting the MXS bits, the result is the same. These same bits appear in both the registers. If the MUXSEL is logic 0 and $\overline{OVRD}$ is logic 1, then, if b7, b6 is "10" then the value on the I-port is passed. when b7 is "00" the value of the SOPRA register is passed on the next IIC stop condition, and when b7 is "01" the value of the SOPRB register is passed on the next IIC stop condition. If MUXSEL is logic 1 and $\overline{OVRD}$ is logic 1, the input lines I0-4 are used to drive the outputs. The above table describes all the combinations.

IIC Interface

The IIC Interface is a standard slave interface. As a slave interface the device will not generate its own clock. Data can be read from and written into the device. Commands for reading and writing the registers are generated by the IIC Master.

START and STOP Conditions

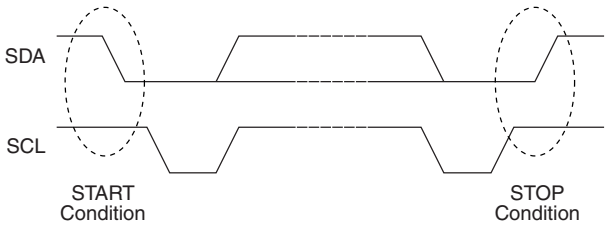


Figure 2. START & STOP Conditions

The IIC protocol uniquely defines START and STOP conditions. A START condition is defined as a HIGH to LOW transition of the SDA signal while SCL is HIGH. A STOP condition is defined as a LOW to HIGH transition of the SDA signal while SCL is HIGH. These are shown in Figure 2.

Device Addressing

The device uses 7-bit IIC addressing.The address has been defined as 1001 110 if the ASEL input is '1' and 0110 111 if the ASEL input is '0'. The address byte is the first byte of data sent after a start condition. This is the only address that this device will respond to. The device will not respond to the general call address 0000 000.

Reading from the Registers

Data can be read from both of the internal registers. All reads are non-destructive and do not change the value in the register or the internal state of the device. When a start condition is received with a read request, both registers can be read out in the following sequence:

(1) SOPRA: Serial Output Port Register A
(2) SPORB: Serial Output Port Register B
(3) PIPR: PORT-I Value

If so desired, only the SOPRA register can be read. This is accomplished by issuing a stop command after the acknowledge bit for the first byte is read. If no stop is issued, the device will output the registers in the above sequence.

Writing to the Registers

Data is written to the SOPR registers through the serial port interface. When a write request is received with the Start Address it is assumed that the intent is to write to the SOPR registers. The value placed in the least 6 significant bits of the register contain the new code to be placed in the SOPR A/B registers. The value of the two most significant bits must contain the address of the destination register SOPRA or SOPRB.

The internal non-volatile latch takes about 10 ms to update its data. The new data is reflected on the outputs after the internal non-volatile latch is updated, if the corresponding select bits (MXSx, $\overline{OVRD}$ and MUXSEL) are set to reflect the state of the non-volatile register.

Register Read Sequence

S	Slave Address	R	A	SOPRA Register	A	SOPRB Register	A	PIPR Register	A	P
S	1001110	1	A	00bbbbbb	A	00bbbbbb	A	00bbbbbb	A	P

Register Write Sequence

S	Slave Address	W	A	SOPRx Register	A	S
S	1001110	0	A	xxbbbbbb	A	S

xx = Register Selection bits (MXSB and MXSA) xx = 00 selects SOPRA, 01 selects SOPRB

Register Write Sequence using Repeated Start Condition

S	Slave Address	R	A	SOPRA Register	A	S	Slave Address	W	A	SOPRx Register	A	P
S	1001110	1	A	00bbbbbb	A	S	1001110	0	A	xxbbbbbb	A	P

Figure 4

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	-0.5V to +6.5V
DC Input Voltage (V_I)	-0.5V to +6.5V
Output Voltage (V_O)	
Outputs 3-stated	-0.5V to +6.5V
Outputs Active (Note 2)	-0.5 to V_{CC}+0.5V
DC Input Diode Current (I_{IK}) V_I < 0V	-50mA
DC Output Diode Current (I_{OK})	
V_O < 0V	-50mA
V_O > V_{CC}	+50mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	±50mA
DC V_{CC} or Ground Current per Supply Pin (I_{CC} or Ground)	±100mA
Storage Temperature Range (T_{STG})	-65°C to +150°C

Recommended Operating Conditions (Note 3)

Power Supply	3.0V to 5.5V
Input Voltage	-0.3V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Output Current I_{OL}	3mA
Free Air Operating Temperature(T_A)	-0°C to +70°C
Minimum Input Edge Rate (dt/dv)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10ns/V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Note 3: Floating or unused pins (inputs or I/O's) must be held HIGH or LOW.

DC Electrical Characteristics (4.5V < V_{CC} ≤ 5.5V unless stated otherwise)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level Input Voltage		V_{CC} x 0.7		V
V_{IL}	Low Level Input Voltage			V_{CC} x 0.3	V
V_{OL}	Low Level Output Voltage	I_{OL} = 100µA I_{OL} = 3mA		0.2 0.4	V
I_{IR}	Input Leakage Current	$V_I = V_{IL}$, V_{CC} = 5.5V	-10	+10	µA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND $V_{CC} \le (V_I, V_O) \le 3.6V$	300	975	µA

DC Electrical Characteristics Extended (3.0V ≤ V_{CC} ≤ 5.5V unless stated otherwise)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level Input Voltage		V_{CC} x 0.7		V
V_{IL}	Low Level Input Voltage			V_{CC} x 0.3	V
V_{OL}	Low Level Output Voltage	I_{OL} = 100µA I_{OL} = 3mA		0.2 0.4	V
V_{OH}	Output High Voltage		2.3	2.5	V
I_{IR}	Input Leakage Current	$V_I = V_{IL}$, V_{CC} = 5.5V	-10	+10	µA
I_{CC}	Quiescent Supply Current	$V_{CC} \le (V_I, V_O) \le 3.6V$	300	975	µA

DC Electrical Characteristics I Port Inputs (V_{CC} = 3.3V)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level Input Voltage	EPV = 2.5V	1.2		V
V_{IL}	Low Level Input Voltage	EPV = 2.5V		0.5	V

AC Characteristics

Symbol	Parameter	$T_A = 0°C$ to $+70°C, C_L = 30pF, R_L = 500\Omega$				Units
		$V_{CC} = 5.0V \pm 0.5V$		$V_{CC} = 3.3V \pm 0.3V$		
		Min	Max	Min	Max	
t_{PHL}	Prop Delay I to Y		50		50	ns
t_{PLH}	Prop Delay I to Y		50		50	ns
t_{PHL}	Prop Delay to Y (from OVRD or MUXSEL)		50		50	ns
t_{PLH}	Prop Delay to Y (from OVRD or MUXSEL)		50		50	ns

IIC AC Characteristics

Symbol	Parameter	$T_A = 0°C$ to $+70°C, C_L = 30pF, R_L = 500\Omega$				Units
		100kHz		400kHz		
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	kHz
T_1	Noise Supression Time Constant		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus must be free before a new Transmission can start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		0.6		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (For a repeated Start Condition)	4.7		0.6		
$t_{HD:DAT}$	Data in Hold Time	0		0		µs
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1000		300	ns
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs

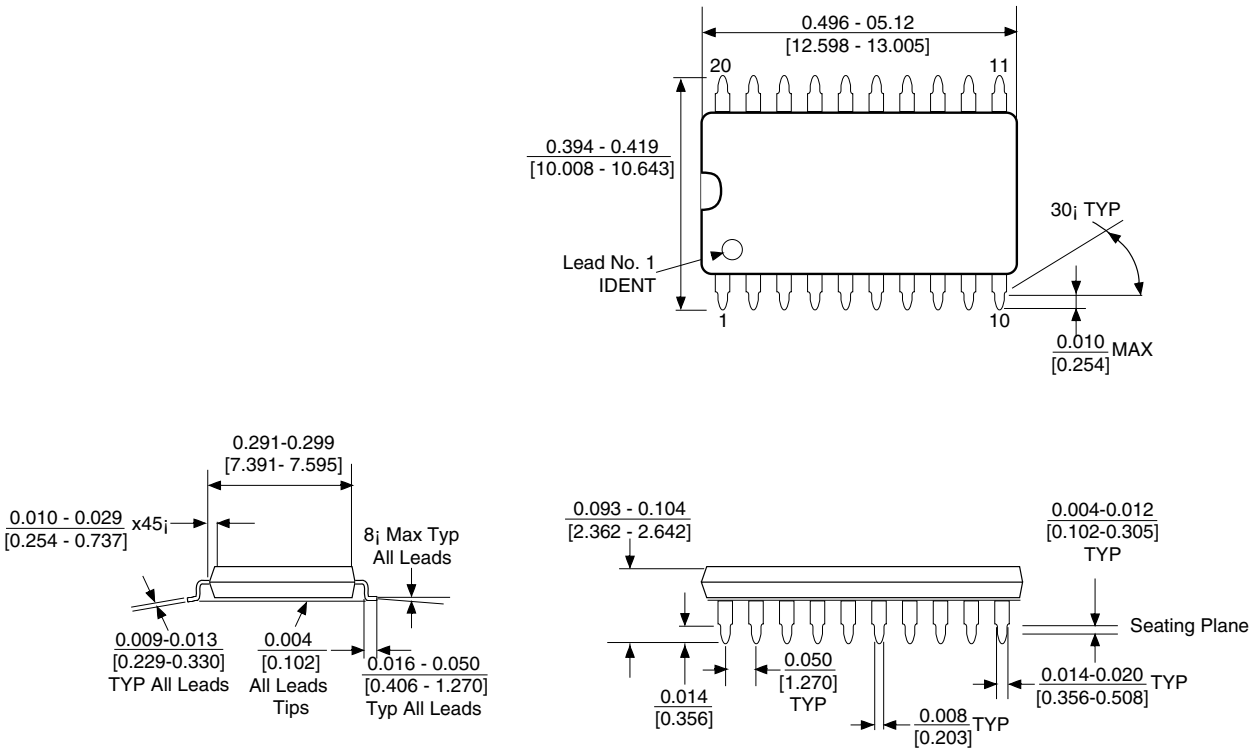
Capacitance ($T_A = +25°C$)

Symbol	Parameter	Conditions	$T_A = +25°C$ Typical	Units
C_{IN}	Input Capacitance (I4-I0)	$V_I = 0V$ or V_{CC}, $V_{CC} = 3.3$ or 5.0	6	pF
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_I = 0V$ or V_{CC}, $V_{CC} = 3.3$ or 5.0	7	pF
C_{OUT}	Output Capacitance (Y4-Y0)		7	pF

Non-Volatile Memory Characteristics

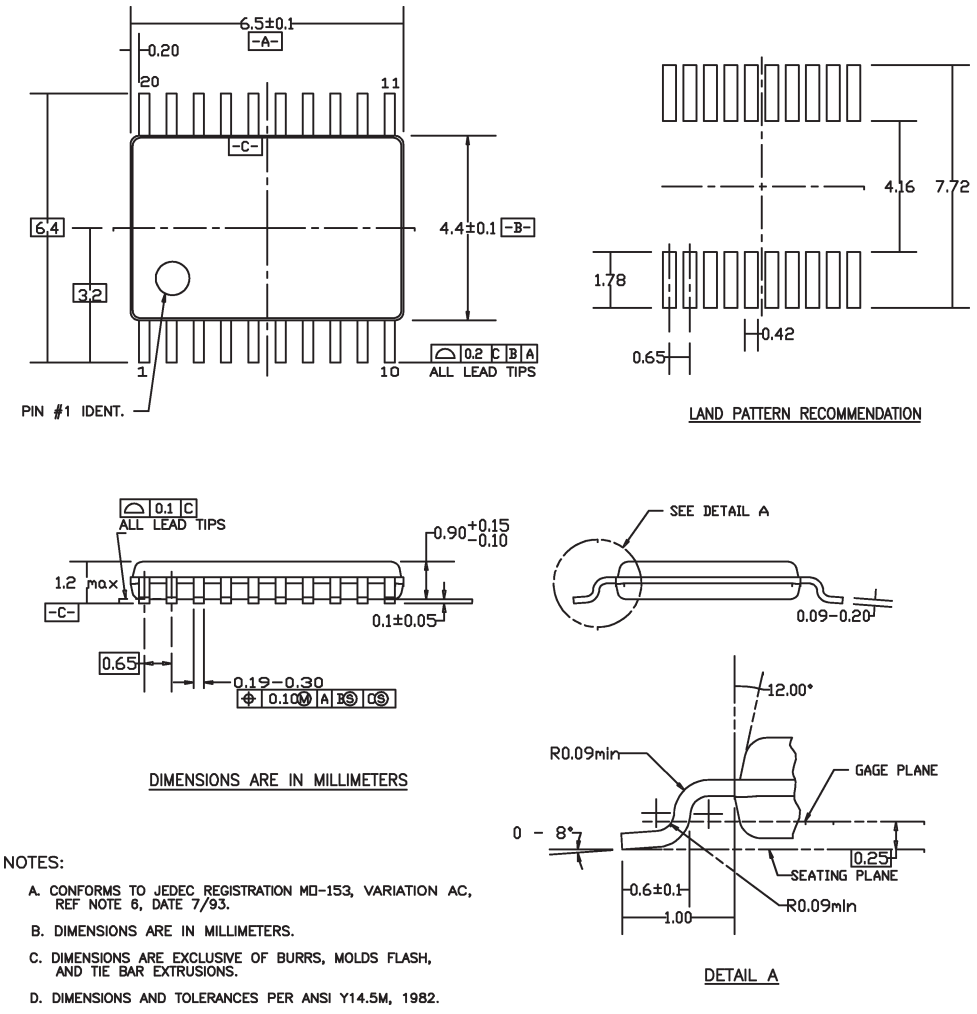
Parameter	Specification
Data Retention	10 years minimum
Number of writes	1,000,000 cycles

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Small Outline Package (M)
Order Number FM3570M20
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

Molded Thin Shrink Small Outline Package (MT)
Order Number FM3570MT20
Package Number MTC20

Life Support Policy

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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