N-CHANNEL SILICON FETS

Symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes with the shield lead connected to the case. The transistors are intended for battery powered equipment and other low current-low voltage applications.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30		V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30		V
Total power dissipation up to T_{amb} = 110 °C	P_{tot}	max.	150		mW
			BFW12	**BFW13**	
Drain current		>	1	0,2	mA
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	<	5	1,5	mA
Gate-source cut-off voltage					
I_D = 0,5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	2,5	1,2	V
Feedback capacitance at f = 1 MHz					
V_{DS} = 15 V; V_{GS} = 0	C_{rs}	<	0,80	0,80	pF
Transfer admittance (common source)					
V_{DS} = 15 V; I_D = 200 μA; f = 1 kHz	$\lvert y_{fs} \rvert$	>	0,5	0,5	mS
Equivalent noise voltage					
V_{DS} = 15 V; I_D = 200 μA					
B = 0,6 to 100 Hz	V_n	<	0,5	0,5	μV

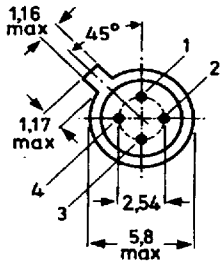
MECHANICAL DATA

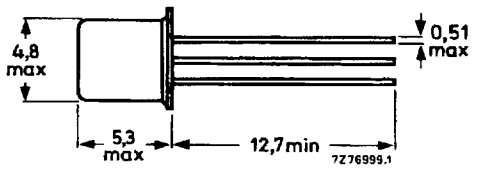
Dimensions in mm

Fig. 1 TO-72.

Pinning

1 = source
2 = drain
3 = gate
4 = shield lead connected to case





Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Drain current	I_D	max.	10	mA
Gate current	I_G	max.	5	mA
Total power dissipation up to T_{amb} = 85 °C	P_{tot}	max.	150	mW
Storage temperature range	T_{stg}	−65 to +	175	°C
Junction temperature	T_j	max.	175	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	590	K/W

CHARACTERISTICS T_j = 25 °C unless otherwise specified

			BFW12	BFW13	
Gate cut-off currents					
$-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	<	0.1	0.1	nA
$-V_{GS}$ = 10 V; V_{DS} = 0; T_j = 150 °C	$-I_{GSS}$	<	0.1	0.1	μA
Drain current [1]					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	1	0.2	mA
		<	5	1.5	mA
Gate-source voltage					
I_D = 50 μA; V_{DS} = 15 V	$-V_{GS}$	>	0.5	0.1	V
		<	2.0	1.0	V
Gate-source cut-off voltage					
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	2.5	1.2	V
y parameters at f = 1 kHz; T_{amb} = 25 °C					
V_{DS} = 15 V; V_{GS} = 0					
Transfer admittance	$\|y_{fs}\|$	>	2.0	1.0	mS
Output admittance	$\|y_{os}\|$	<	30	10	μS
V_{DS} = 15 V; I_D = 500 μA					
Transfer admittance	$\|y_{fs}\|$	>	1.5	-	mS
Output admittance	$\|y_{os}\|$	<	10	-	μS
V_{DS} = 15 V; I_D = 200 μA					
Transfer admittance	$\|y_{fs}\|$	>	0.5	0.5	mS
Output admittance	$\|y_{os}\|$	<	5	5	μS
f = 1 MHz; T_{amb} = 25 °C					
V_{DS} = 15 V; V_{GS} = 0					
Input capacitance	C_{iss}	<	5	5	pF
Feedback capacitance	C_{rs}	<	0.80	0.80	pF
Equivalent noise voltage					
V_{DS} = 15 V; I_D = 200 μA; T_{amb} = 25 °C B = 0.6 to 100 Hz	V_n	<	0.5	0.5	μV

[1]) Measured under pulsed conditions.