intel®

80C49-7/80C39-7
CHMOS SINGLE-COMPONENT 8-BIT MICROCOMPUTER

- ■ 80C49-7 Low Power Mask Programmable ROM
- ■ 80C39-7 Low Power, CPU only

- ■ Pin-to-pin Compatible with Intel's 8049AH/8039AHL

- ■ 1.36 μsec Instruction Cycle. All Instructions 1 or 2 Cycles

- ■ Ability to Maintain Operation during AC Power Line Interruptions

- ■ Exit Idle Mode with an External or Internal Interrupt Signal

- ■ Battery Operation

- ■ 3 Power Consumption Selections
  —Normal Operation: 12 mA @ 11 MHz @ 5V
  —Idle Mode: 5 mA @ 11 MHz @ 5V
  —Power Down: 2 μA @ 2.0V

- ■ 11 MHz, TTL Compatible Operation:
  V_{CC} = 5V ± 10%
  CMOS Compatible Operation;
  V_{CC} = 5V ± 20%

Intel's 80C49-7/80C39-7 are low power, CHMOS versions of the popular MCS*-48 HMOS family members. CHMOS is a technology built on HMOS II and features high resistivity P substrate, diffused N well, and scaled N and P channel devices. The 80C49-7/80C39-7 have been designed to provide low power consumption and high performance.

The 80C49-7 contains a 2K x 8 program memory, a 128 x 8 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to an on-board oscillator and clock circuits. For systems that require extra capability, the 80C49-7 can be expanded using CMOS external memories and MCS*-80 and MCS*-85 peripherals. The 80C39-7 is the equivalent of the 80C49-7 without program memory on-board.

The CHMOS design of the 80C49-7 opens new application areas that require battery operation, low power standby, wide voltage range, and the ability to maintain operation during AC power line interruptions. These applications include portable and hand-held instruments, telecommunications, consumer, and automotive.
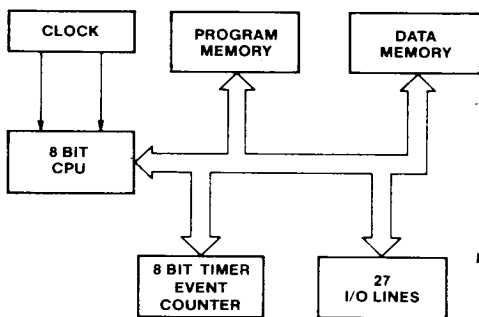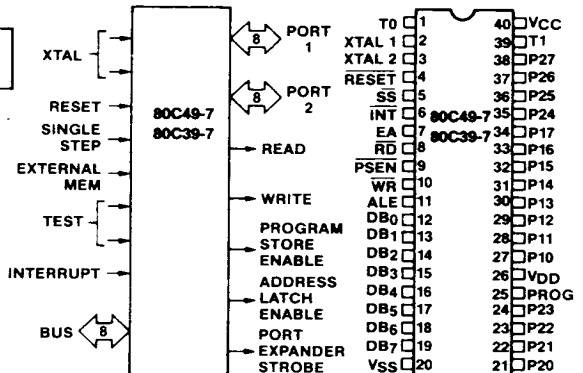

Figure 1.
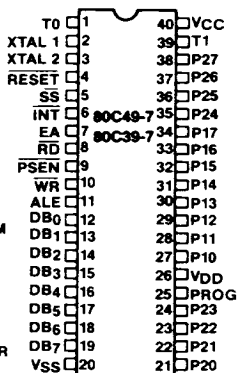Block Diagram

Figure 2.
Logic Symbol

Figure 3.
Pin Configuration

Table 1. Pin Description

Symbol	Pin No.	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	Low Power standby pin
V_{CC}	40	Main power supply; +5V during operation.
PROG	25	Output strobe for 82C43 I/O expander.
P10–P17 Port 1	27–34	8-bit quasi-bidirectional port.
P20–P23	21–24	8-bit quasi-bidirectional port.
P24–P27 Port 2	35–38	P20–P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.
DB0–DB7 BUS	12–19	True bidirectional port which can be written or read synchronously using the RD, WR strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, RD, and WR.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNTo. T0 can be designated as a clock output using ENT0 CLK instruction.
T1	39	Input pin testable using the JT1, and JNT1 instructions.

Symbol	Pin No.	Function
		Can be designated the timer/counter input using the STRT CNT instruction.
INT	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low) Interrupt must remain low for at least 3 machine cycles for proper operation.
RD	8	Output strobe activated during a BUS read. Can be used to enable data onto toe bus from an external device. Used as a read strobe to external data memory. (Active low)
RESET	4	Input which is used to initialize the processor. (Active low) (Non TTL V_{IH})
WR	10	Output strobe during a bus write. (Active low) Used as write strobe to external data memory.
ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
PSEN	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low)
SS	5	Single step input can be used in conjunction with

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Table 1. Pin Description (Continued)

Symbol	Pin No.	Function
SS (Con't)		ALE to "single step" the processor through each instruction (Active low)
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing

Symbol	Pin No.	Function
		and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL V_{IH})
XTAL2	3	Other side of crystal input.

IDLE MODE DESCRIPTION

The 80C49-7, when placed into Idle mode, keeps the oscillator, the internal timer and the external interrupt and counter pins functioning and maintains the internal register and RAM status.

To place the 80C49-7 in Idle mode, a command instruction (op code 01H) is executed. To terminate Idle mode, a reset must be performed or interrupts must be enabled and an interrupt signal generated. There are two interrupt sources that can restore normal operation. One is an external signal applied to the interrupt pin. The other is from the overflow of the timer/counter. When either interrupt is invoked, the CPU is taken out of Idle mode and vectors to the interrupt's service routine address. Along with the Idle mode, the standard MCS®-48 power-down mode is still maintained.

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Table 2. Instruction Set

Accumulator

Mnemonic	Description	Bytes	Cycles
ADD A, R	Add register to A	1	1
ADD A, @R	Add data memory to A	1	1
ADD A, # data	Add immediate to A	2	2
ADDC A, R	Add register with carry	1	1
ADDC A, @R	Add data memory with carry	1	1
ADDC A, # data	Add immediate with carry	2	2
ANL A, R	And register to A	1	1
ANL A, @R	And data memory to A	1	1
ANL A, # data	And immediate to A	2	2
ORL A, R	Or register to A	1	1
ORL A @R	Or data memory to A	1	1
ORL A, # data	Or immediate to A	2	2
XRL A, R	Exclusive or register to A	1	1
XRL A, @R	Exclusive or data memory to A	1	1
XRL, A, # data	Exclusive or immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal adjust A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1

Input/Output

Mnemonic	Description	Bytes	Cycles
IN A, P	Input port to A	1	2
OUTL P, A	Output A to port	1	2
ANL P, # data	And immediate to port	2	2
ORL P, # data	Or immediate to port	2	2
INS A, BUS	Input BUS to A	1	2
OUTL BUS, A	Output A to BUS	1	2
ANL BUS, # data	And immediate to BUS	2	2
ORL BUS, # data	Or immediate to BUS	2	2
MOVD A, P	Input expander port to A	1	2
MOVD P, A	Output A to expander port	1	2
ANLD P, A	And A to expander port	1	2
ORLD P, A	Or A to expander port	1	2

Registers

Mnemonic	Description	Bytes	Cycles
INC R	Increment register	1	1
INC @R	Increment data memory	1	1
DEC R	Decrement register	1	1

Branch

Mnemonic	Description	Bytes	Cycles
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ R, addr	Decrement register and skip	2	2
JC addr	Jump on carry = 1	2	2
JNC addr	Jump on carry = 0	2	2
JZ addr	Jump on A zero	2	2
JNZ addr	Jump on A not zero	2	2
JT0 addr	Jump on T0 = 1	2	2
JNT0 addr	Jump on T0 = 0	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on T1 = 0	2	2
JF0 addr	Jump on F0 = 1	2	2
JF1 addr	Jump on F1 = 1	2	2
JTF addr	Jump on timer flag	2	2
JNI addr	Jump on INT = 0	2	2
JBb addr	Jump on accumulator bit	2	2

Subroutine

Mnemonic	Description	Bytes	Cycles
CALL addr	Jump to subroutine	2	2
RET	Return	1	2
RETR	Return and restore status	1	2

Flags

Mnemonic	Description	Bytes	Cycles
CLR C	Clear carry	1	1
CPL C	Complement carry	1	1
CLR F0	Clear flag 0	1	1
CPL F0	Complement flag 0	1	1
CLR F1	Clear flag 1	1	1
CPL F1	Complement flag 1	1	1

Table 2. Instruction Set (Continued)

Data Moves

Mnemonic	Description	Bytes	Cycles
MOV A, R	Move register to A	1	1
MOV A, @R	Move data memory to A	1	1
MOV A, # data	Move immediate to A	2	2
MOV R, A·	Move A to register	1	1
MOV @R, A	Move A to data memory	1	1
MOV R, # data	Move immediate to register	2	2
MOV @R, # data	Move immediate to data memory	2	2
MOV A, PSW	Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1
XCH A, R	Exchange A and register	1	1
XCH A, @R	Exchange A and data memory	1	1
XCHD A, @R	Exchange nibble of A and register	1	1
MOVX A, @R	Move external data memory to A	1	2
MOVX @R, A	Move A to external data memory	1	2
MOVP A, @A	Move to A from current page	1	2
MOVP3 A, @A	Move to A from page 3	1	2

Timer/Counter

Mnemonic	Description	Bytes	Cycles
MOV A, T	Read timer/counter	1	1
MOV T, A	Load timer/counter	1	1
STRT T	Start timer	1	1
STRT CNT	Start counter	1	1
STOP TCNT	Stop timer/counter	1	1
EN TCNTI	Enable timer/counter interrupt	1	1
DIS TCNTI	Disable timer/counter interrupt	1	1

Control

Mnemonic	Description	Bytes	Cycles
EN I	Enable external interrupt	1	1
DIS I	Disable external interrupt	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
SEL MB0	Select memory bank 0	1	1
SEL MB1	Select memory bank 1	1	1
ENT0 CLK	Enable clock output on T0	1	1

Mnemonic	Description	Bytes	Cycles
NOP	No operation	1	1
IDL	Select Idle Operation	1	1

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . 0°C to 70°C
Storage Temperature . . . . . . −65°C to +150°C
Voltage On Any Pin With Respect
   to Ground . . . . −0.5V to V_{CC} +1V
Maximum Voltage On Any Pin
   With Respect to Ground 7V
Power Dissipation . . . . 1.0 Watt

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

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IARACTERISTICS: (T_A = 0°C to 70°C; V_{CC} = V_{DD} = 5V ± 20%; $|V_{CC} - V_{DD}| \leq 1.5V$; V_{SS} = 0V)

	Parameter	Min	Typ	Max	Unit	Test Conditions
	Input Low Voltage (All Except X1, $\overline{RESET}$)	−.5		.18 V_{CC}	V	
	Input Low Voltage X1, $\overline{RESET}$	−5		.13 V_{CC}	V	
	Input High Voltage (All Except XTAL1, $\overline{RESET}$)	0.2 V_{CC} + 1.2		V_{CC}	V	
I	Input High Voltage (X1, $\overline{RESET}$)	.7 V_{CC}		V_{CC}	V	
_	Output Low Voltage (BUS)			.6	V	I_{OL} = 2.0 mA
_1	Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)			.6	V	I_{OL} = 1.8 mA
L2	Output Low Voltage (PROG)			.6	V	I_{OL} = 1.0 mA
)L3	Output Low Voltage (All Other Outputs)			.6	V	I_{OL} = 1.6 mA
)H	Output High Voltage (BUS)	.75 V_{CC}			V	I_{OH} = −400 µA
)H1	Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	.75 V_{CC}			V	I_{OH} = −100 µA
OH2	Output High Voltage (All Other Outputs)	2.4 3.0			V	I_{OH} = −40 µA I_{OH} = −20 µA
_1	Input Leakage Current (T1, $\overline{INT}$, EA)			±5	µA	$V_{SS} \leq V_{IN} \leq V_{CC}$
LI1	Input Leakage Current (P10–P17, P20–P27, $\overline{SS}$)			−500	µA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{LO}	Output Leakage Current (BUS, TO) (High Impedance State)			±5	µA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{LR}	Input Leakage Current ($\overline{RESET}$)	−10		−300	µA	$V_{SS} \leq V_{IN} \leq V_{IH1}$
I_{PD}	Power Down Standby Current			2	µA	V_{DD} = 2.0V $\overline{RESET} \leq V_{IL}$

I_{CC} Active Current (mA)

V_{CC}	4V	5V	6V
1 MHz	2.5	3.3	4.0
6 MHz	5	6.8	8.5
11 MHz	9	12	15

I_{CC} Idle Current (mA)

V_{CC}	4V	5V	6V
1 MHz	1.7	2.0	2.2
6 MHz	2	3	4
11 MHz	3.5	4.8	6

Absolute Maximum Unloaded Current

I_{CC} Test Conditions:

I_{CC} Active
All outputs disconnected
T1, $\overline{INT}$, SS, T0 connected to HIGH (V_{IH})
EA, $\overline{RST}$ connected to LOW (V_{IL})
XTAL1 External Drive
  Rise Time = 10 ns, Fall Time = 10 ns
XTAL2 No connection
V_{IH} = V_{CC} − 0.5V
V_{IL} = V_{SS} + 0.5V

I_{CC} Idle
All outputs disconnected
XTAL1 External Drive
  Rise Time = 10 ns, Fall Time = 10 ns
XTAL2 No connection
V_{IH} = V_{CC} − 0.5V
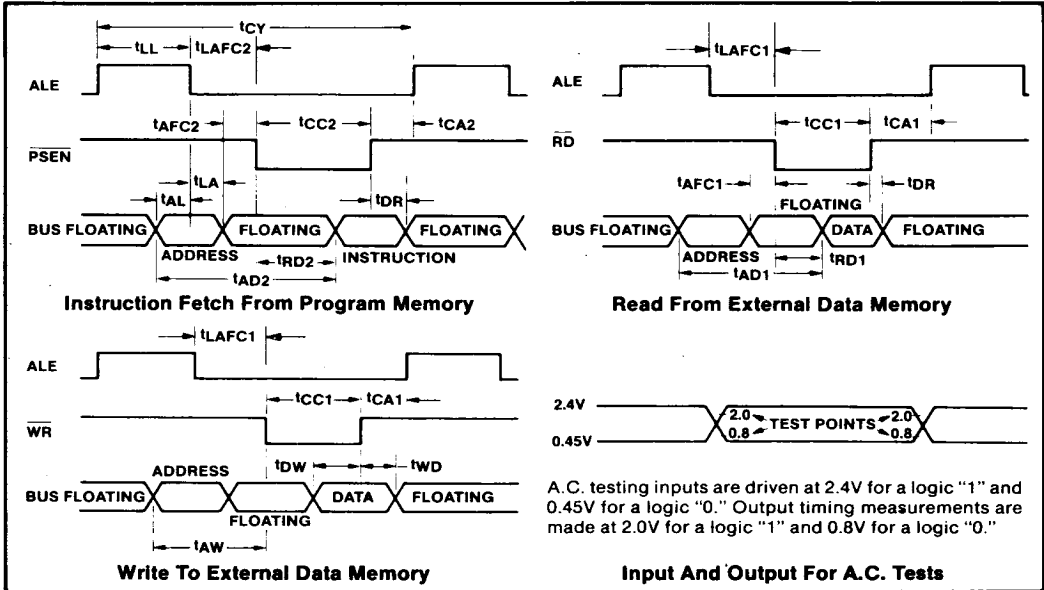V_{IL} = V_{SS} + 0.5V

A.C. CHARACTERISTICS: ($T_A = 0°C$ to $70°C$; $V_{CC} = V_{DD} = 5V \pm 20\%$; $|V_{CC} - V_{DD}| \leqslant 1.5V$; $V_{SS} = 0V$)

Symbol	Parameter	f (t) (Note 3)	11 MHz Min	11 MHz Max	Unit	Conditions (Note 1)
t	Clock Period	1/xtal freq	90.9	1000	ns	(Note 3)
t_{LL}	ALE Pulse Width	3.5t−170	150		ns	
t_{AL}	Addr Setup to ALE	2t−110	70		ns	(Note 2)
t_{LA}	Addr Hold from ALE	t−40	50		ns	
t_{CC1}	Control Pulse Width ($\overline{RD}$, $\overline{WR}$)	7.5t−200	480		ns	
t_{CC2}	Control Pulse Width ($\overline{PSEN}$)	6t−200	350		ns	
t_{DW}	Data Setup before $\overline{WR}$	6.5t−200	390		ns	
t_{WD}	Data Hold after $\overline{WR}$	t−50	40		ns	
t_{DR}	Data Hold ($\overline{RD}$, $\overline{PSEN}$)	1.5t−30	0	110	ns	
t_{RD1}	$\overline{RD}$ to Data in	6t−170		350	ns	
t_{RD2}	$\overline{PSEN}$ to Data in	4.5t−170		190	ns	
t_{AW}	Addr Setup to $\overline{WR}$	5t−150	300		ns	
t_{AD1}	Addr Setup to Data ($\overline{RD}$)	10.5t−220		730	ns	
t_{AD2}	Addr Setup to Data ($\overline{PSEN}$)	7.5t−220		460	ns	
t_{AFC1}	Addr Float to $\overline{RD}$, $\overline{WR}$	2t−40	140		ns	(Note 2)
t_{AFC2}	Addr Float to $\overline{PSEN}$	.5t−40	10		ns	(Note 2)
t_{LAFC1}	ALE to Control ($\overline{RD}$, $\overline{WR}$)	3t−75	200		ns	
t_{LAFC2}	ALE to Control ($\overline{PSEN}$)	1.5t−75	60		ns	
t_{CA1}	Control to ALE ($\overline{RD}$, $\overline{WR}$, $\overline{PROG}$)	t−65	25		ns	
t_{CA2}	Control to ALE ($\overline{PSEN}$)	4t−70	290		ns	
t_{CP}	Port Control Setup to $\overline{PROG}$	1.5t−80	50		ns	
t_{PC}	Port Control Hold to $\overline{PROG}$	4t−260	100		ns	
t_{PR}	$\overline{PROG}$ to P2 Input Valid	8.5t−120		650	ns	
t_{PF}	Input Data Hold from $\overline{PROG}$	1.5t	0	140	ns	
t_{DP}	Output Data Setup	6t−290	250		ns	
t_{PD}	Output Data Hold	1.5t−90	40		ns	
t_{PP}	$\overline{PROG}$ Pulse Width	10.5t−250	700		ns	
t_{PL}	Port 2 I/O Setup to ALE	4t−200	160		ns	
t_{LP}	Port 2 I/O Hold to ALE	1.5t−120	15		ns	
t_{PV}	Port Output from ALE	4.5t+100		510	ns	
t_{OPRR}	T0 Rep Rate	3t	270		ns	
t_{CY}	Cycle Time	15t	1.36	15.0	μs	

Notes:

1. Control Outputs CL = 80pF
   BUS Outputs CL = 150pF

2. BUS High Impedance
   Load 20pF

3. f(t) assumes 50% duty cycle on X1, X2. Max clock period is for a 1 MHz crystal input.

WAVEFORMS

Instruction Fetch From Program Memory

Read From External Data Memory

Write To External Data Memory

A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0." Output timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0."

Input And Output For A.C. Tests

PORT 1/PORT 2 TIMING

SUGGESTED ROM VERIFICATION ALGORITHM FOR CHMOS DEVICES ONLY

	C48	C49	C50
A10	0	ADDR	ADDR
A11	0	0	ADDR

$V_{CC} = V_{DD} = +5V$

$V_{SS} = 0V$

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